Pentacene Integrated Thin-film Transistors and Circuits

by

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Abstract

Organic semiconductors offer the potential of large-area, mechanically flexible electronics due to their low processing temperatures. We have developed a near-room-temperature ($\leq$ 95°C) process flow to fabricate pentacene integrated organic thin-film transistors (OTFTs) compatible with plastic substrates such as polyethylene terephthalate (PET).

Integration of inkjet printed organic photoconductors (OPDs) based on titanyl pthalocyanine with OTFTs is demonstrated for the first time in an integrated process. Using the OTFT as a switch in series with an OPD, a pixel circuit was designed and measured, in addition to a proof-of-concept 4x4 active matrix imager. The individual pixels were measured to have a responsivity of $6x10^{-5}$ A/W, and a pixel on/off conductance ratio of 880, both at an irradiance of 5 mW/cm^2. The imager uses a 25 V power supply and was shown to correctly image a "T" pattern after 1st order calibration.

A model for the current-voltage characteristics based upon amorphous silicon models was implemented in MATLAB to investigate design trade-offs in organic digital circuits. A dual threshold voltage process is suggested to enable area-efficient zero-V_{GS} current sources. The area and power savings of this approach is discussed compared to a single V_T process. We also motivate the necessity for lowering the power supply, both for area savings and improvement in circuit lifetime due to reduction in bias stress effects.

A process flow for a dual V_T OTFT technology, enabled using two gate metals, is presented. By using a low work function metal (aluminum) and a high work function metal (platinum), we can obtain two threshold voltage devices. Devices were measured to be nominally identical, shifted by a V_{SG} which we call the ΔV_T. A ΔV_T of 0.6 V was consistently observed over multiple wafer lots. This is the first demonstration of modification of OTFT V_T by changing the gate work function.

Area-minimized digital logic designed in the dual V_T technology was demonstrated with a 3 V supply, the lowest supply reported for integrated OTFTs. In addition, we report some of the first analog organic integrated circuits, including a differential pair with differential gain of 23 dB and common-mode rejection ratio (CMRR) of 23 dB. A two-stage uncompensated operational amplifier was fabricated and measured to have an open-loop gain of 36 dB and unity gain frequency of 7.5 Hz. The op-amp has a unity gain-bandwidth product of 473 Hz while dissipating < 2 nW with a 5 V supply. The comparator uses 5 nW of power, and has an input offset of 200 mV.

We show the frequency response of the op-amp and comparator are dominated by parasitic overlap capacitances. The parasitics of the zero-V_{GS} load limits frequency response, and technological improvements to increase operating frequency are suggested. We motivate a self-aligned process flow, which uses a high optical density gate to serve as a mask layer. A backside exposure patterns the source/drain layer. It is demonstrated that the parasitic capacitances can be reduced by almost an order of magnitude, from 1 fF/μm to 0.15 fF/μm. A method to improve carrier mobility is also presented. These process improvements have the potential to improve the switching speeds of organic circuits by more than two orders of magnitude.

Thesis Supervisor: Charles G. Sodini
Title: LeBel Professor

To the faculty, students, and staff of the Microsystems Technology Laboratories.

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Chapter 1 Introduction

Thin-film transistors (TFTs) are transistors made by depositing a thin-film semiconductor layer on top of an arbitrary substrate, rather than using a semiconductor wafer as both the channel material and mechanical support. Early work by Lilienfeld, Brody, Heil and later William Shockley laid the foundation for TFTs in the 1930's and 40's, but it was not until Paul Weimer's work in 1962 that thin-film transistors of reasonable performance were demonstrated [1]. Weimer described a shadow-mask fabricated TFT using a channel layer of cadmium sulfide (CdS) and a gate dielectric of silicon monoxide (SiO) with impressive open circuit voltage gain and switching speed.

Since his seminal paper on CdS TFTs, other materials such as cadmium selenide (CdSe) and tellurium (Te) have been investigated as potential channel materials, but hydrogenated amorphous silicon (a-Si:H) has become the most popular TFT material since its demonstration in the 1970's [2]. To date, a-Si:H, and to a lesser extent polycrystalline (poly-Si), are the only TFT channel materials which have achieved widespread commercial adoption to this date.

TFT technologies have a number of advantages compared to their single crystal counterparts, even though their carrier mobilities are significantly lower. Thin-films of semiconductors can be easily deposited by chemical vapor deposition (CVD) or sputtering, enabling thin-film transistors to be fabricated over areas much larger than 300 mm - at present the largest diameter Si wafer in commercial production. At the time of this writing, a-Si:H TFTs are fabricated on Gen 10 glass (2.85 m x 3.05 m) for liquid crystal displays (LCDs) backplanes.

While it is true that the amorphous or polycrystalline semiconductors used for TFTs exhibit substantially lower mobilities, there are many applications which do not require the performance achieved by single crystal metal oxide semiconductor field-effect transistors

(MOSFETs). The active matrix backplanes of LCDs and x-ray imagers are two applications perfectly suited for TFTs, since large area is required with only moderate switching speed.

Future generations of large-area electronics will be integrated into roll-able displays, flexible imagers, and conformal displays and sensors. All these applications require fabrication on mechanically flexible, plastic substrates such as polyethylene teraphthalate (PET). Amorphous and poly-silicon devices are incompatible with the constrained thermal budgets of these polymer substrates. Organic semiconductor-based devices can achieve reasonable performance at processing temperatures within these thermal budgets. The following section will discuss organic semiconductors whose development holds the promise for large-area and flexible electronics due to their near-room-temperature processing capabilities.

1.1 Organic Semiconductors

1.1.1 Organic Molecules

Organic semiconductors are carbon based molecules which exhibit semiconducting behavior. Although a physical derivation of molecular orbital theory and the electronic structure of organic molecules is beyond the scope of this thesis, a brief summary describing the origin of semiconduction in organic molecules is described below.

Organic semiconductors owe their behavior to alternating single and double carbon-carbon bonds. The alternating bond structure is known as conjugation, and the sp^2 hybridization in the bonding leads to delocalization of electrons on the molecule and π-bonding.

Figure 1-1 pictures a molecule of butadiene, illustrating the alternating single and double bonds. The electronic energy levels of this system can be found by treating the system as a particle-in-a-box, or a particle in an infinite potential well. This well-studied quantum mechanical problem yields solutions of distinct, quantized energy levels, whose spacing is determined by the degree of physical confinement in the box. In this case, the confinement is the length of the molecule. The energy levels in this system are given by the following equation, where m is the mass of the particle, L the length of the potential well, and $\hbar$ the reduced Planck's constant. For the case of butadiene, we use the mass of an electron, $m=9.1\text{x}10^{-31}$ kg, and L= 0.4 nm [3].

$$E_n = \frac{\hbar^2 \pi^2 n^2}{2mL^2} \tag{1-1}$$

As an example, the π-bonding energy levels for butadiene will be found analytically, and these states will be populated by the available amount of electrons (four). Filling two electrons of opposite spin for level, we see that the 2nd level (n=2) is fully populated, and the energy level above it (n=3) is empty. This second level is known as the highest occupied molecular orbital (HOMO), and the level directly above it, the lowest unoccupied molecular orbital (LUMO).

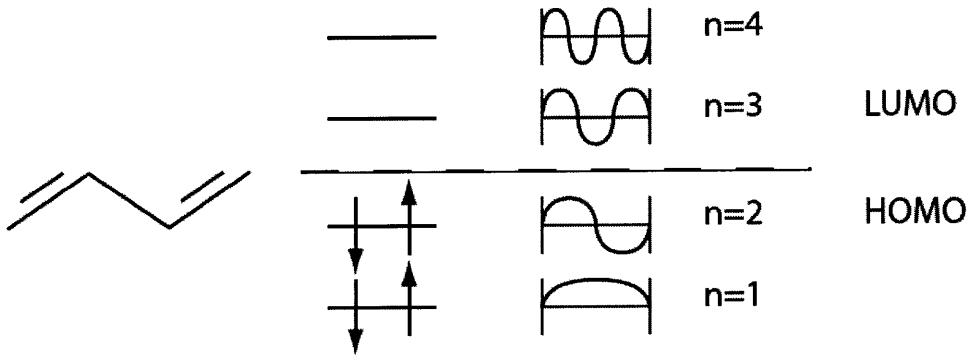

Figure 1-1: Butadiene molecule, and its energy levels [3].

These two energy levels are analogous to the valence and conduction band energies in classical semiconductors, and will be essential in determining both the optical and electronic properties of the molecule.

If the size of the conjugated molecule increases, the HOMO-LUMO gap decreases. In other words, the energy levels decrease in spacing as the level of confinement is reduced.

Material	PFEO	Experimental value
Benzene	6.3eV	6.0eV
Napthalene	3.8eV	4.3eV
Anthracene	2.7eV	3.3eV
Tetracene	2.1eV	2.6eV
Pentacene	1.7eV	2.1eV

Figure 1-2: HOMO-LUMO gap for various acenes [3]. Perimeter free electron orbital (PFEO) model compared with experimental data.

This trend can be seen in a class of organic molecules called acenes. The acenes are of particular interest because they contain the fundamental structure of popular organic electronic materials such as graphene, carbon nanotubes, and buckminster fullerene (C_{60}) [4]. Napthalene consists of two benzene rings, anthracene three benzene rings, and so forth.

Pentacene, which consists of five fused benzene rings, has a HOMO-LUMO gap of 2.1 eV. Pentacene will be revisited later in the section.

1.1.2 Organic Thin-Films

By placing a number of organic molecules next to each other, one creates an organic thin-film. If these molecules are highly ordered and form crystal grains, the film is called poly-crystalline. If there is no long range spatial order or alignment to the molecules in the film, it is referred to as amorphous. A schematic of these two thin-film morphologies is seen in Figure 1-3.

Figure 1-3: Poly-crystalline organic film, showing well ordered grain structure (left). Amorphous organic film, indicating no long range spatial order (right).

Whether the film is amorphous or poly-crystalline, the organic molecules in the film only weakly interact with each other via Van der Waals forces. Therefore, the movement of charge through an organic thin-film is described by hopping transport in which a charge hops from one localized state (one molecule) to another. Because of the weak interaction, the carrier mobility in organic thin-films is orders of magnitude lower than covalently bonded semiconductors like silicon. Poly-crystalline organic thin-films typically have higher mobilities compared to amorphous organic films. Since charge transport strongly depends on intermolecular distance, densely packed films will have improved mobilities.

In silicon and other crystalline, covalent semiconductors, there is strong wavefunction overlap from electronic site to site. This strong interaction leads to charge transfer by band transport through delocalized states, and higher carrier mobilities. The following table summarizes the differences between organic semiconductor thin-films and covalently bonded inorganic semiconductors.

	Molecular semiconductors	Covalent semiconductors
Lattice interaction	Van der Waals (10^{-3} – 10^{-1} eV)	Covalent (2-4 eV)
Carrier mobility	≤1 cm^2/Vs	100~10,000 cm^2/Vs
Mean free path	Short (~lattice constant)	Long (~10^2-10^3 x lattice constant)
Carrier effective mass	Large (10^2-10^3 x electron mass)	Small (< 1x electron mass)
Charge transport type	Hopping	Band
Melting point	Low	High
Mechanical strength	Low	High
Compressibility	High	Low

Table 1-1: Comparing molecular to covalent inorganic semiconductor crystals. After [5,6].

1.1.3 Motivation for Organic TFTs

Although organic thin-films have poor charge transport properties due to weak molecular interaction, molecular thin-films do have their advantages. The Van der Waals forces mean that organic molecules can be evaporated from bulk at low temperatures, enabling low temperature deposition processes. Also, since each bond in the molecule is satiated, organic semiconductors do not have any dangling bonds which would need to be passivated by some means of processing or annealing. These two properties enable organics to be processed in ways impossible for other semiconductors. Indeed, organics offer exciting new opportunities as the active material for TFTs due to their unique processing capabilities.

Comparatively, other TFT semiconductors like a-Si:H and poly-Si require processing steps of 300°C or higher in order to incorporate hydrogen to passivate dangling silicon bonds in the bulk semiconductor and at the semiconductor-dielectric interface. Organic semiconductors, however, can be simply evaporated from a powder form at low temperature (~200°C), or put in solvent and inkjet printed, while keeping the substrate near room temperature. The lack of dangling bonds omits the need for high temperature anneals.

Thus, the low temperature processing conditions of organic TFTs allow them to be fabricated on a wide range of mechanically flexible, low glass transition temperature (≤120°C) substrates such as PET or polyethylene naphthalate (PEN). Secondly, the ability of organic molecules to be dispersed in solvents and inkjet printed offers a new paradigm for semiconductor fabrication – i.e. one of additive, rather than subtractive, patterning. The benefit is 100% materials efficiency, and the processing of semiconductor devices without the need for photolithography or chemical and plasma etches.

1.2 Organic TFTs

Over the last thirty years, the electronic performance of organic TFTs has seen tremendous improvement. The first field-effect behavior in an organic metal-insulator-semiconductor structure was reported in 1983 by *Ebisawa et al.* at NTT [7,8]. Although a TFT was not demonstrated, this study documented insulated gate control of a polyacetylene film. This was followed in 1986 by the first organic thin-film transistor, published by *Tsumura et al.* at Mitsubishi Chemical in 1986 [9]. This device consisted of a highly doped silicon wafer which was used as the gate, below a thermal oxide and polythiophene film. The mobility was found to be ~ 10^{-5} cm^2/Vs.

Since Tsumura's publication in 1986, the carrier mobility in organic TFTs has increased five orders of magnitude, to state-of-the-art OTFTs exhibiting around 1 cm^2/Vs [10]. The dramatic increase in mobility has much to due with the discovery of the molecule pentacene. Shown below, pentacene ($C_{22}H_{14}$) is an aromatic hydrocarbon consisting of five fused benzene rings.

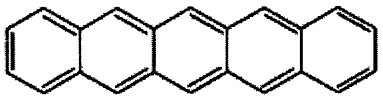

Figure 1-4: Structure of pentacene [11].

Pentacene is currently the favorite organic material for thin-film transistors. Like most organic semiconductors, conduction in pentacene favors hole transport, and hole mobilities of 1 cm^2/Vs have been reported, on par with electron mobilities observed in a-Si:H [10]. In addition, pentacene's relative environmental robustness makes it even more appealing.

Although a number of TFT fabrication processes and device structures have been published, all organic TFTs work in the same manner. In the next section, the basic operation of an organic TFT will be described.

1.3 Operation & Characterization of Organic TFTs

Whether the channel layer is amorphous silicon or pentacene, thin-film transistors operate significantly different than MOSFETs.

The standard MOSFET is operated in inversion. When a gate to source voltage (V_{GS}) sufficiently greater than the threshold voltage (V_T) is applied, an inversion layer of minority carriers is formed at the semiconductor-oxide interface, with a concentration (cm^{-3}) greater than that of the background doping density. When a drain to source voltage (V_{DS}) is applied, current conducts through the inversion layer between two highly doped source and drain contacts.

Thin-film transistors, however, are operated in accumulation. Pictured here is a cross section view of a pentacene TFT and its corresponding circuit symbol.

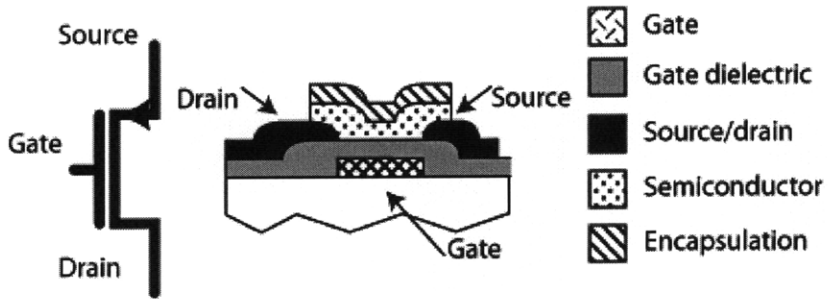

Figure 1-5: Pentacene TFT cross section.

The cross section depicts what is called a bottom gate, co-planar TFT. Co-planar indicates that the gate, source, and drain are in contact with the same surface of the semiconductor. This device is also called a bottom contact geometry, since the source and drain contact the bottom of the semiconductor. It may also be referred to as "inverted" since the gate is at the bottom of the structure.

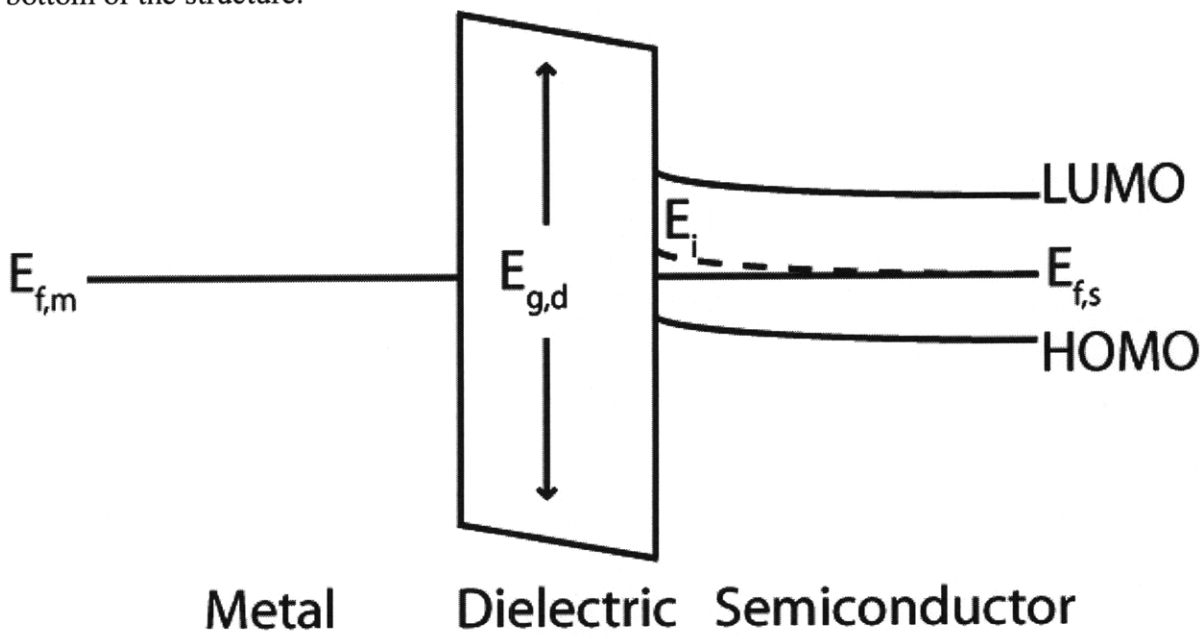

Figure 1-6: Metal-dielectric-semiconductor system for V_{SG}=0 V. The work function of the metal is greater than the potential in the semiconductor. $E_{g,d}$ is the band gap of the dielectric.

Shown in Figure 1-6 are the energy levels of the metal-insulator-semiconductor system, when no external field is applied. In the above picture, we assume there is no fixed charge, and that the Fermi level of the semiconductor, $E_{f,s}$, is less than the Fermi level of the metal, $E_{f,m}$. This is quite common, since high work function materials such as gold are typically used for the gate. The picture is very similar to that of a silicon metal-oxide-semiconductor

(MOS) system, except the conduction and valence bands are replaced with the LUMO and HOMO, respectively.

$V_{SG} \leq V_{OFF}$

When a negative source to gate voltage (V_{SG}) less than V_{OFF} is applied, no measurable electrons or holes are induced in the channel, and no measurable current flows between the source and the drain regardless of the source to drain voltage (V_{SD}). This regime is called "cutoff".

$V_{OFF} < V_{SG} < V_T$

As we apply a more positive V_{SG}, the semiconductor surface potential moves towards the HOMO and a layer of holes begins to accumulate at the semiconductor-dielectric interface. A current from source to drain (I_{SD}) can now be measured. Holes flow from drain to source by hopping between localized states.

The magnitude of the current varies rapidly with a change in V_{SG} since the current is dominated by diffusion current. This regime is called "subthreshold". The subthreshold regime is quantified by measuring at the subthreshold slope (S), i.e., how much of an increase in V_{SG} is necessary to achieve a decade increase in I_{SD}.

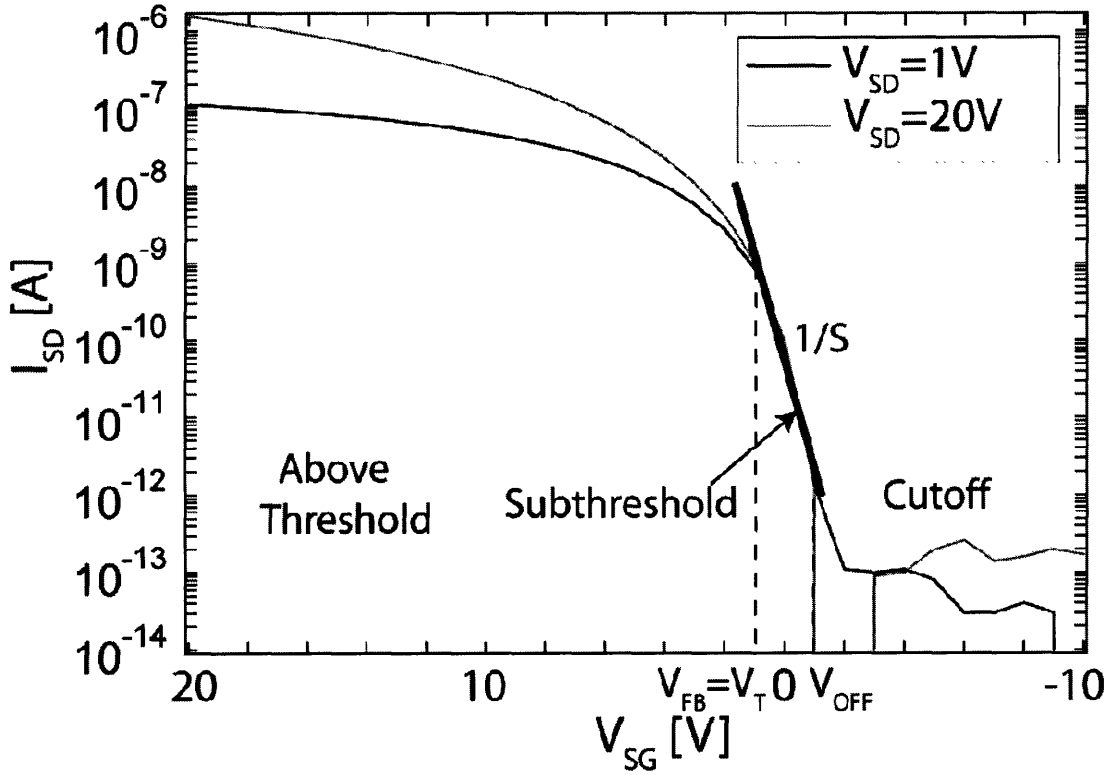

Figure 1-7: Transfer curves in linear (V_{SD}=1 V), and saturation (V_{SD}=20 V). W/L=200 μm/25 μm.

$V_{SG} \geq V_T$

The point at which the drain current deviates from a linear fit, plotted semilog, is called the threshold voltage (V_T), and marks the transition from exponential diffusion current to drift current. We use the term threshold voltage since it is the term most often used in literature, but this voltage actually refers to the flatband voltage (V_{FB}), since these devices operate in accumulation.

As we apply a more positive V_{SG} and pass V_T, we move "above threshold". At a low V_{SD}, we are in the linear, or triode regime, and at a sufficiently high V_{SD} ($V_{SD} \geq V_{SG}+V_T$), saturation. These different regimes can be seen in I_{SD} vs. V_{SD}, known as the output characteristics.

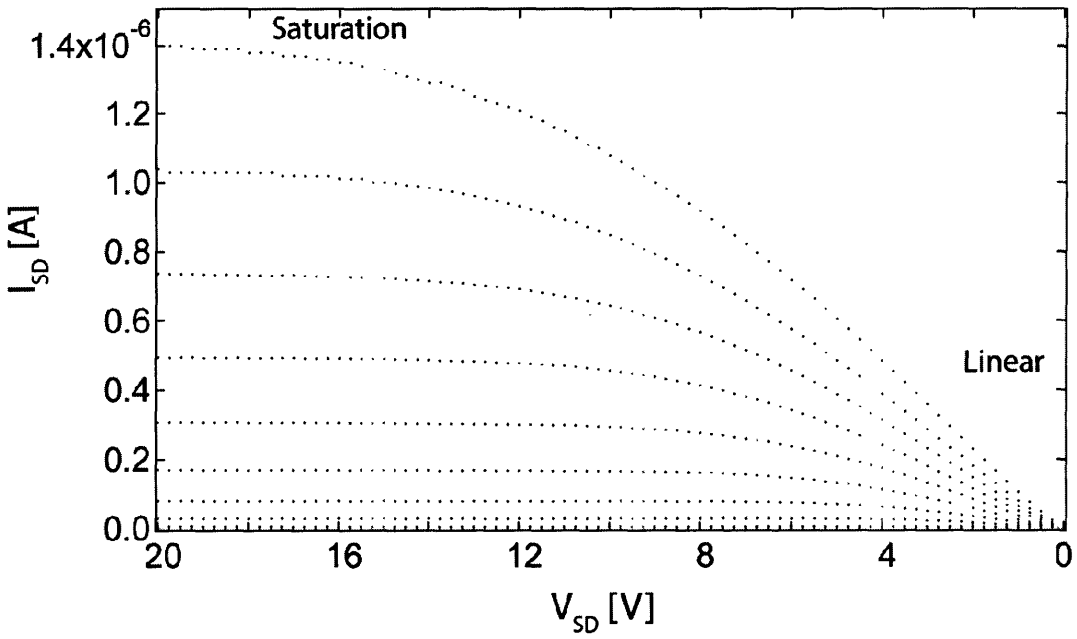

Figure 1-8: Typical measured output curves, V_{SG} stepped from 0 V to 20 V with 2 V steps. W/L= 200 μm /25 μm.

The following table shows typical parameters for OTFTs fabricated at MIT using a photolithographic process. These parameters are obtained from the above current-voltage characteristics, in addition to quasi-static capacitance-voltage (QSCV) measurements.

Parameter	Value
$I_{G,leak}$/Width	5 fA/μm
$I_{DS,leak}$/Width	2.1 fA/μm
S	0.6 V/dec
V_{OFF}	4 V
V_T	-1 V
On/off ratio ("on" V_{SG}=20V, V_{SD}=20V, "off" V_{SG}=0V, V_{SD}=20V)	$9x10^6$
I_{on} (V_{SG}=20V, V_{SD}=20V)/Width	11.4 nA/μm
C_{ox}	22 nF/cm^2
$R_{contact}$	$5.7*10^2$ MΩ μm
μ	0.024 cm^2/Vs
λ	0.05 V^{-1}

Table 1-2: Typical transistor parameters for a W=1000 μm, L=5 μm device.

V_{OFF}, as explained earlier, is the voltage at which the drain current equals the gate leakage current. $R_{contact}$ is obtained by taking current-voltage characteristics in the linear regime for devices of various channel lengths, and fixed widths. By plotting the resistance of each

device versus channel length, we can find the contact resistance by extrapolating the linear fit to L=0. This technique is known as the transmission line method (TLM) [12]. This is illustrated in Figure 1-9.

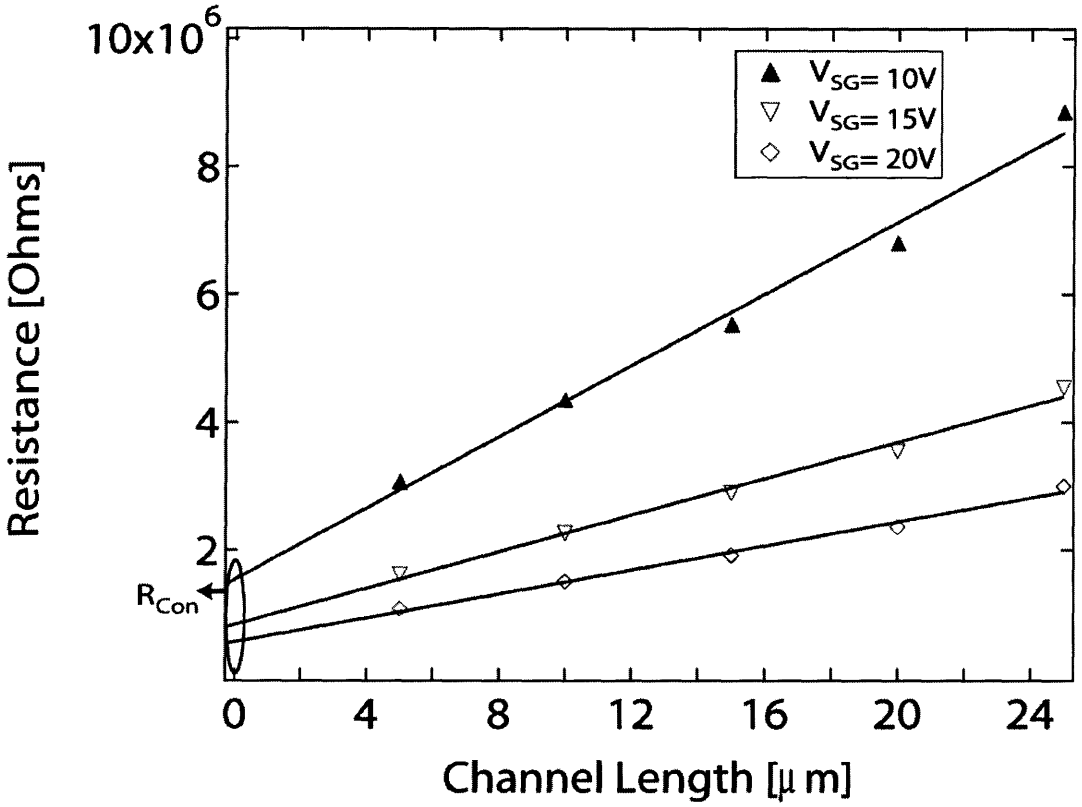

Figure 1-9: Resistance versus channel length for various V_{SG}, W=1000 μm.

The gate-voltage dependent contact resistance has been widely reported in literature. This behavior is due to the Schottky diode like metal-organic source/drain contacts.

$R_{contact}$ is also necessary to accurately extract the mobility. We follow the method of *Ryu et al.* which calculates the mobility by the following equations [13].

$$\mu = \frac{v}{E} \quad , \quad v = \frac{I_{SD}}{WQ}$$
$$E = \frac{V_{SD} - I_{SD}R_{contact}}{L} \tag{1-2}$$

W and L are the width and length of the OTFT, v the carrier velocity, E the electric field, and Q is the sheet charge density (C/cm^2), which is found by integrating the QSCV.

The electric field is constant across the channel in the linear regime ($E=V_{SD}/L$), however, due to contact resistance, one must subtract the voltage dropped over the contacts to obtain the actual voltage drop over the channel.

As expected for a device made of an amorphous semiconductor, the mobility is gate voltage dependent, and increases with increasing overdrive, seen in Figure 1-10. This behavior has been studied in literature and is due to the large density of traps in the bandgap [14].

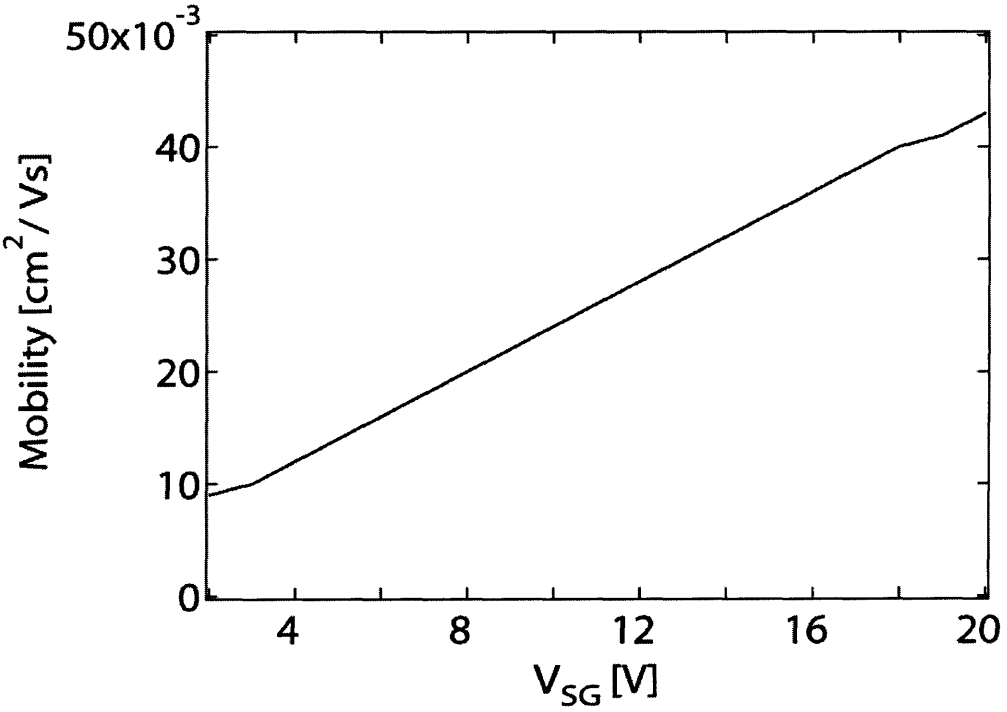

Figure 1-10: Mobility versus V_{SG} with contact resistance accounted, W=250 μm, L=25 μm.

A disordered semiconductor film like pentacene has a significant density of states in the bandgap. A schematic of the density of states versus energy is shown below.

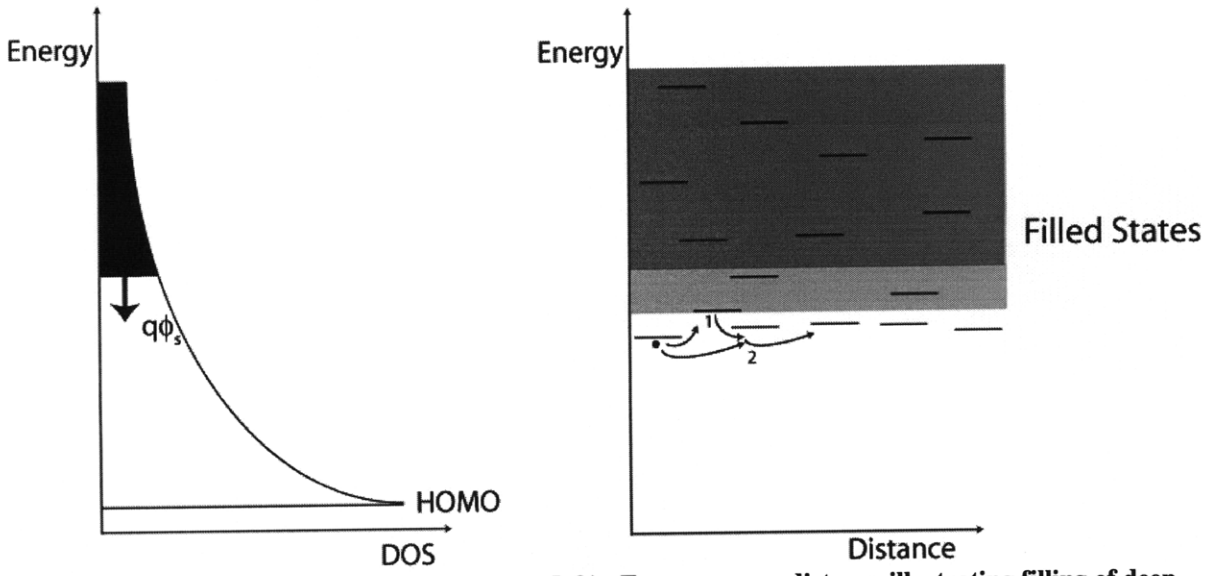

Figure 1-11: Density of states versus energy (left). Energy versus distance illustrating filling of deep traps with increasing overdrive (right). With a higher gate overdrive, deep trap state 1 is now filled, and the carrier hops to site 2 instead. Site 2 is a shallower trap, and a carrier can more easily hop from this site to the next.

As the gate overdrive is increased, the potential in the pentacene, φ_s, moves closer to the HOMO. By doing so, more traps are populated with carriers. Therefore, the average trap energy level seen by a carrier is lower as the semiconductor potential moves closer to the HOMO. The observed result is higher carrier mobility. The mobility in OTFTs is typically modeled by assuming that carriers at the HOMO level have a mobility of μ_o and all other carriers have a mobility of 0. The effective mobility μ_{eff}, is equal to the concentration of carriers thermally promoted to the HOMO [14].

$$\mu_{eff} = \mu_o e^{-(E_{HOMO}-q\phi_s)/kT} \tag{1-3}$$

The presence of bandgap states also affects the subthreshold slope. Figure 1-12 shows a typical transfer curve, with the subthreshold region highlighted. Unlike a typical silicon MOSFET whose slope is constant, the subthreshold slope in OTFTs varies with V_{SG}.

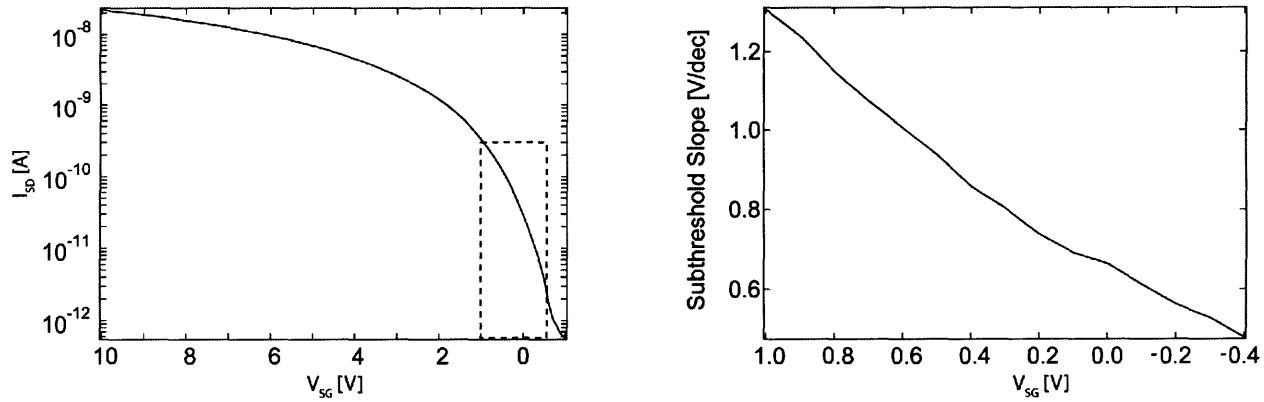

Figure 1-12: Transfer curve of W/L = 200 μm/25 μm device and its subthreshold slope.

This behavior is understood if one considers the density of states in the bandgap. Figure 1-13 shows a plot of the energy versus the density of states (DOS) for two semiconductors, one with a large density of bandgap states, and the other with a small density. When a voltage is applied to the gate of a transistor with capacitance C_g, charge $Q=C_gV$ will be induced in the semiconductor. Figure 1-13 indicates that the density of states will dictate how large a change in the semiconductor potential, φ_s, will occur from this gate voltage.

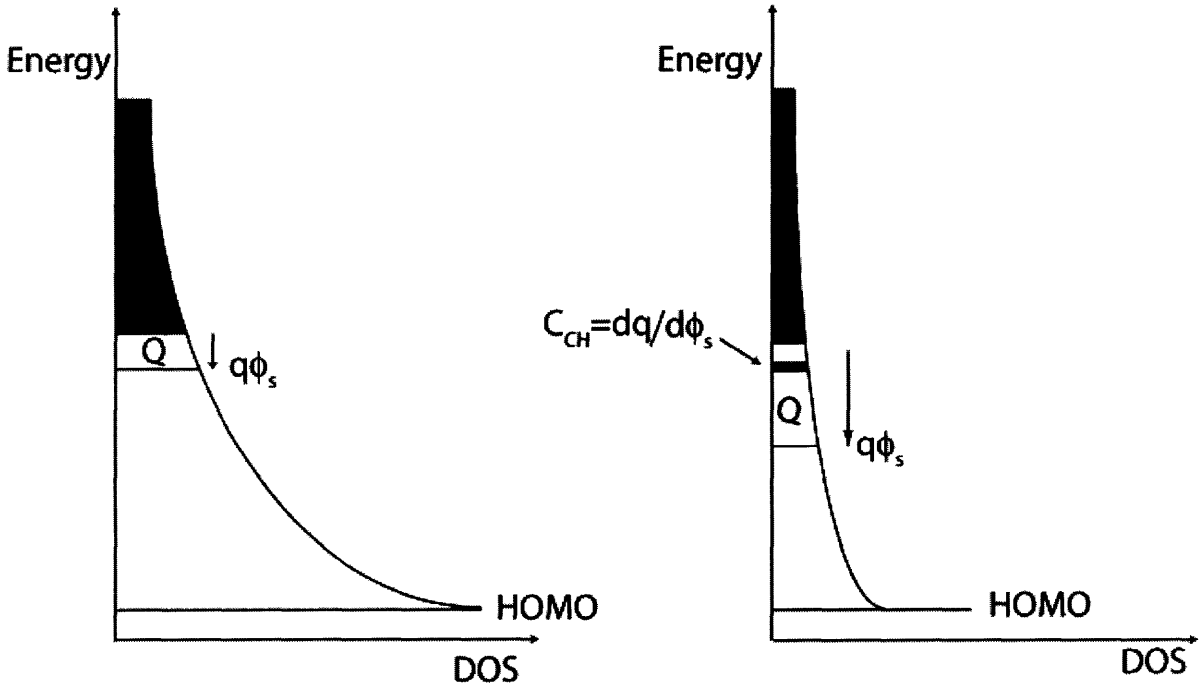

Figure 1-13: Energy versus density of states (DOS) for two devices. The device on the left has significantly more bandgap states than the device on the right. The quantity Q is the same for both [15].

The change in charge in the semiconductor with respect to a change in the semiconductor potential, is given by the channel capacitance, $C_{CH} = dq/d\phi_s$. With this knowledge, one can draw a simple capacitor divider circuit, illustrating the effect of the density of states. In this

circuit, C_g is the OTFT gate capacitance, φ_s the semiconductor potential, and C_{CH} the capacitance associated with the density of states. Since the density of states changes with energy, C_{CH} is not constant, and is evaluated at the position of φ_s. Because the density of states increases with energy, C_{CH} will increase as the potential moves closer to the HOMO. One can therefore write the subthreshold slope as follows.

$$S = \frac{C_g}{C_g + C_{CH}(\phi_s)} 60mV \tag{1-4}$$

The device with fewer bandgap states will have a smaller C_{CH} and subthreshold slope – i.e. its current will rise more sharply with an increase in V_{SG}.

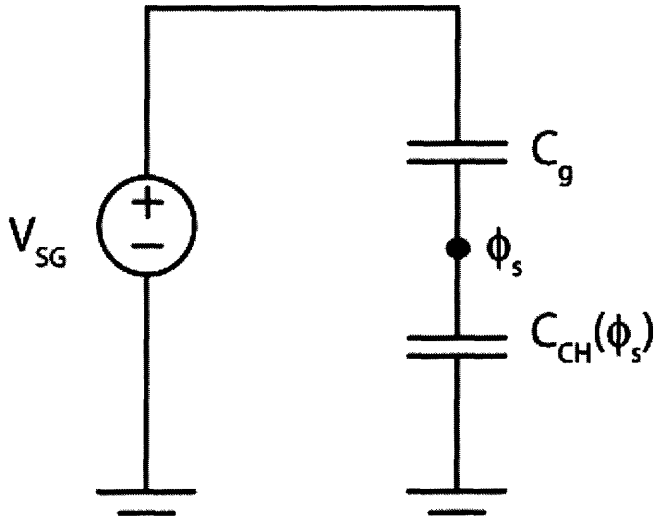

Figure 1-14: Capacitor divider resulting from the density of states. The value of C_{CH} is dependent on the position of the semiconductor potential [15].

1.3.1 Small Signal Characteristics

The previous section described the large signal characteristics of OTFTs. In most analog circuits, voltage or current signals are typically applied that are much smaller in magnitude compared to the DC bias conditions. Because these signals are small relative to the bias, one can linearize the transistor around the bias point.

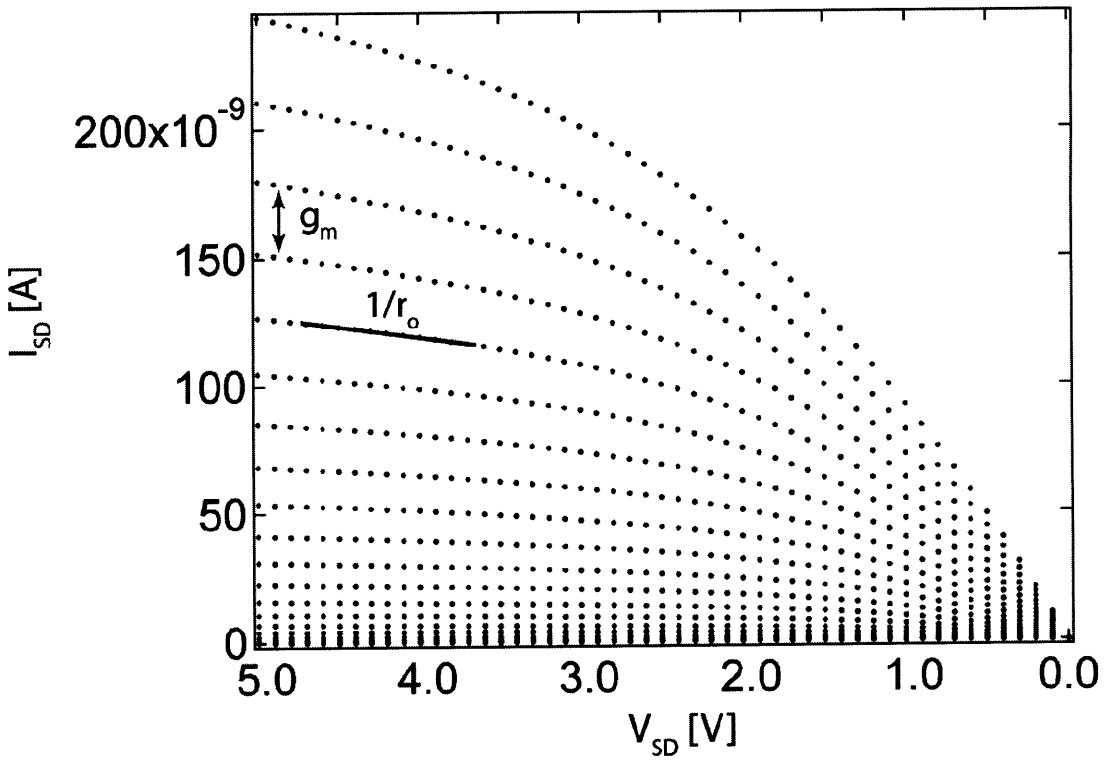

Figure 1-15: Output curves of device with W/L=515 μm/5 μm, illustrating extraction of g_m and r_o. Lambda=0.05 V^{-1}. V_{SG} stepped from 0 to 5 V with 0.5 V increments.

The OTFT is linearized by taking the derivative of the drain current equation, with respect to the small signal quantities. Specifically, we are interested in finding the change in current due to a small change in the gate voltage and the change in current due to a small change in the drain to source voltage.

$$g_m = \frac{\Delta I_{SD}}{\Delta V_{SG}}$$
$$\frac{1}{r_o} = \frac{\Delta I_{SD}}{\Delta V_{SD}} \qquad (1\text{-}5)$$

The transconductance, g_m, and the output resistance, r_o, are illustrated in Figure 1-15. For OTFTs, these small signal quantities are obtained by performing the derivatives in Equation 1-5 on measured data. Although these values are always calculated from data, there are two noteworthy trends in OTFTs to mention.

The drain current in saturation for a MOSFET is shown in Equation 1-6, where $K = \frac{W}{L} C_{ox}$.

$$I_{SD} = \frac{1}{2} K\mu (V_{SG} + V_T)^2 \tag{1-6}$$

The transconductance, g_m, can be found by taking the derivative of Equation 1-6 with respect to V_{SG}. In silicon MOSFETs, the mobility is a function of V_{SG}, and decreases with increasing gate voltage due to scattering at the semiconductor-insulator interface [16]. However, when deriving the g_m for silicon devices, it is conventional to assume the mobility to be constant, i.e. $d\mu / dV_{SG} = 0$. With this assumption, one obtains the classical expression for g_m, Equation 1-7.

$$g_m = \sqrt{2K\mu I_{SD}} = K\mu (V_{SG} + V_T) \tag{1-7}$$

OTFTs, however, exhibit increasing mobility with gate overdrive, as discussed earlier. Here, we do not neglect the derivative of mobility with respect to V_{SG}.

$$\begin{aligned} g_m &= \frac{1}{2} K \frac{d\mu}{dV_{SG}} (V_{SG} + V_T)^2 + K\mu (V_{SG} + V_T) \\ g_m &= \frac{d\mu}{dV_{SG}} \frac{I_{SD}}{\mu} + \sqrt{2K\mu I_{SD}} \end{aligned} \tag{1-8}$$

The left-hand terms in Equation 1-8 are both positive. We see that Equation 1-8 simplifies to Equation 1-7 if one sets $d\mu / dV_{SG} = 0$.

Figure 1-16 plots the measured g_m versus I_{SD}.

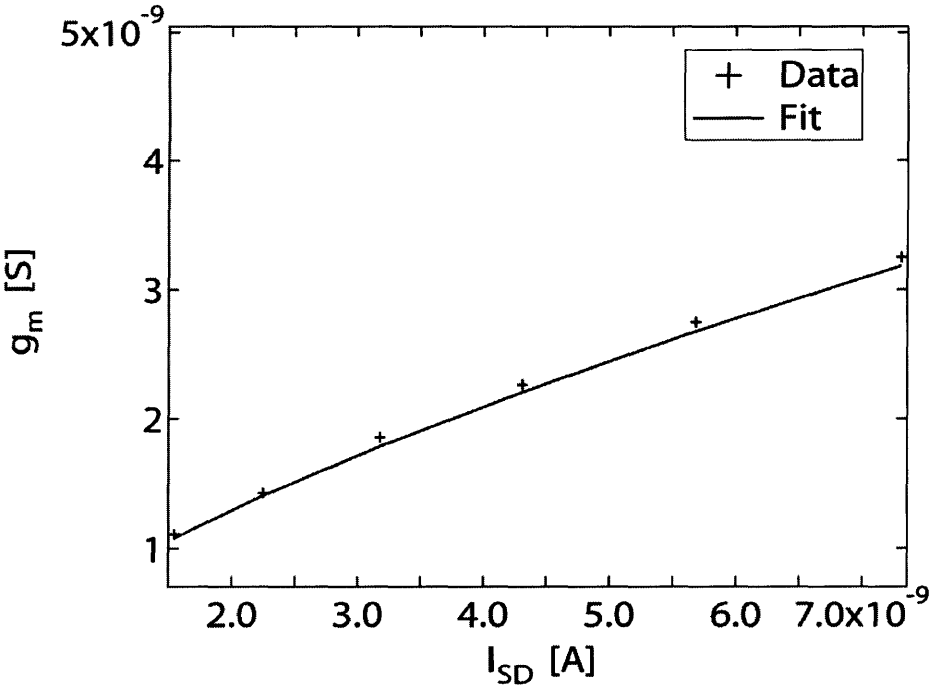

Figure 1-16: Data and fit of g_m vs I_{SD}. $G_m \sim I_{SD}^{0.69}$,

The output resistance is extracted by taking the change in drain current with a change drain voltage while the device is in saturation. As is the case for MOSFETs, a $1/I_{SD}$ relationship is observed. R_o is given by Equation 1-9. Lambda is typically around 0.05 V^{-1} for a 5 μm length device.

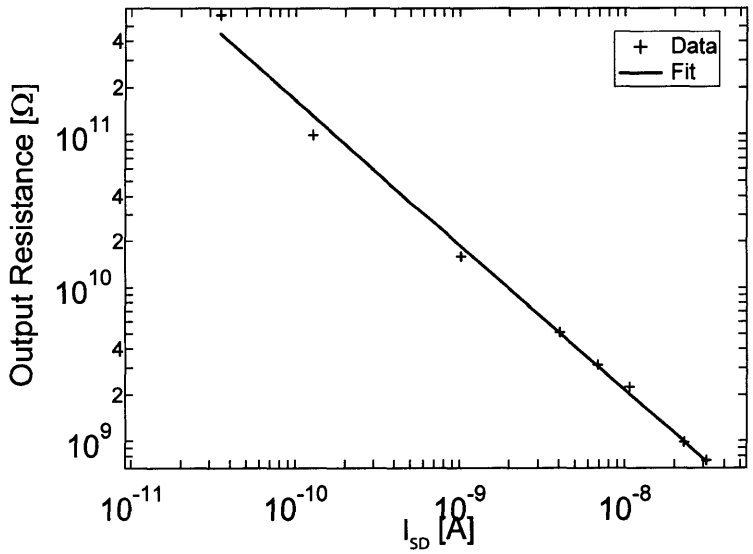

Figure 1-17: Data and fit of r_o vs I_{SD}. $Ro \sim I_{SD}^{-.95}$ for 515 μm/5 μm device, λ=0.05 V^{-1}.

$$r_o = \frac{1}{\lambda I_{SD}} \tag{1-9}$$

As is the case in MOSFETs, lambda is inversely proportional to the channel length, L. This relationship is pictured in Figure 1-18. It is difficult to accurately measure lambda for long channel lengths, as the ΔI from lambda is comparable with the ΔI from stressing the device during measurement. Therefore, the extracted lambda for long channel (>20 μm) devices is underestimated.

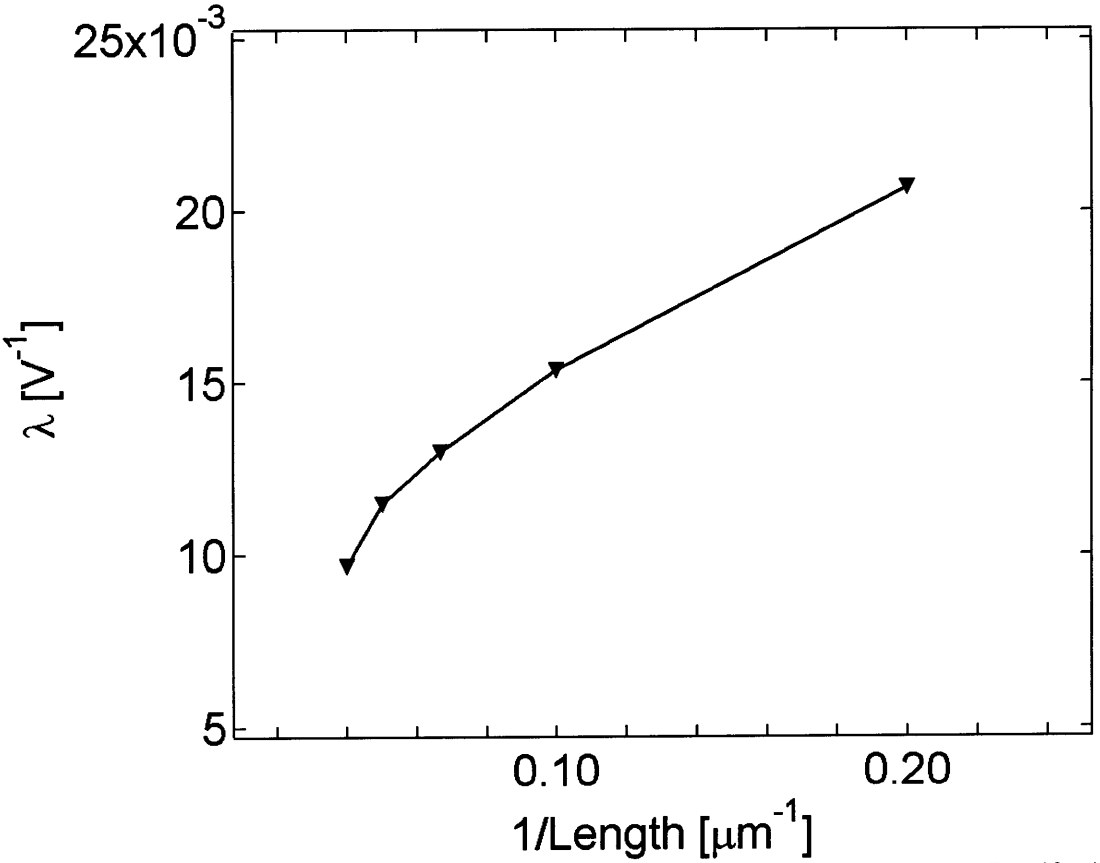

Figure 1-18: Measured data of λ vs. channel length. All devices of W=1000 μm, I_{SD}=10 μA.

1.4 Processing Organic TFTs

A review of OTFT literature shows a number of process flows used fabricate organic thin-film transistors. In general, we can divide these processes into three categories: shadow-masked, solution processed, and photolithographic. These three processes will be briefly summarized, noting their advantages and disadvantages. Particular emphasis will be placed on the photolithographic process.

1.4.1 Shadow Mask

The simplest technique for fabricating OTFTs uses shadow masks to pattern the source/drain and active regions. Shadow masks are thin metal sheets, typically stainless steel, in which the desired pattern is machined. By placing the mask in contact with the substrate during deposition steps, the desired pattern is transferred. For OTFTs, the gate can be patterned by shadow masks, or a highly doped silicon wafer can serve as the global gate. The process flow for top contact shadow-masked OTFTs as processed at MIT is shown below.

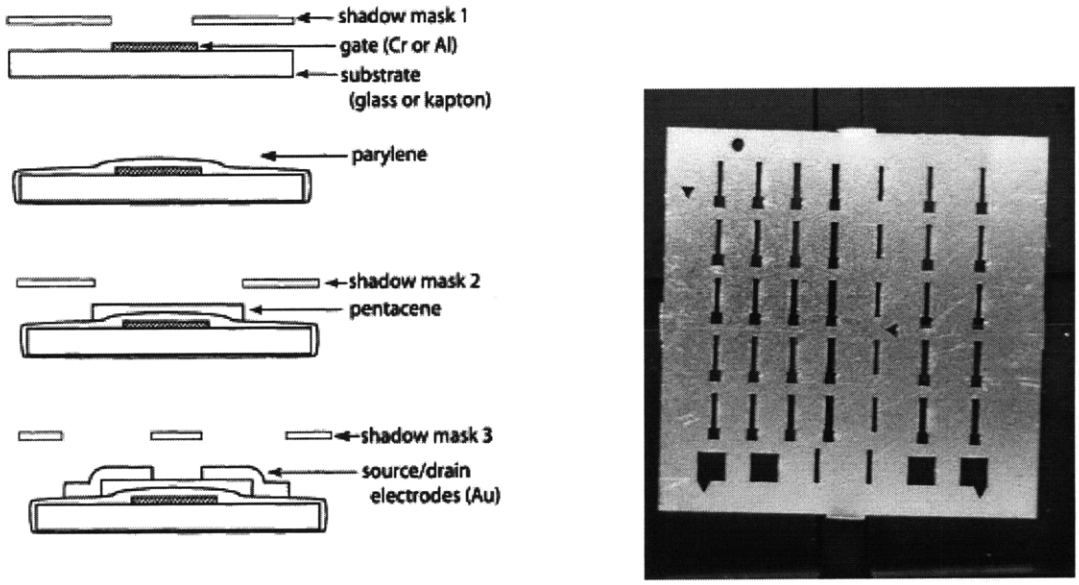

Figure 1-19: Shadow-mask process at MIT [11]. Photograph of 20 mm x 20 mm metal shadow mask used to pattern gate layer.

There are a number of advantages and disadvantages to using shadow masks to pattern OTFTs. In general, it requires fewer steps than photolithographic processing, allowing quick fabrication of test devices. Shadow-masking also allows the fabrication of a top-contact geometry, which has been shown to result in improved semiconductor microstructure and electronic performance compared to bottom-contact geometries, which must be used in photolithographic fabrication [17]. A shadow-masked process also does not use solvents, which have been shown to induce morphological changes in pentacene [18].

However, shadow masks only provide coarse resolution of ~20 μm at best. Not only does this limit the minimum channel length, it also increases the gate to source/drain overlap, increasing parasitic capacitances. Lastly, since the masks are made from thin metal sheets, they cannot be scaled to large areas as the metal will bow, limiting the minimum feature size

attainable for a given shadow-mask size. Therefore, shadow-mask patterning cannot be used to fabricate large-area electronics [19].

1.4.2 Solution Processed

Since most organic semiconductors can be solvated quite easily, the resulting semiconductor solutions can be patterned by spin-casting or drop-casting. The latter offers the potential for low-cost manufacturing of printed electronics due to the process' materials and energy efficiency, and ambient processing conditions.

Inkjet printed OTFTs typically use polymeric materials such as polythiophene instead of small molecule semiconductors. Pentacene is not easily solvated, and the molecule must be chemically modified in order to enable solution processing. 6,13-bis(triisopropyl-silylethynyl) pentacene (TIPS pentacene) has been demonstrated in spin-cast TFTs with mobilities on par with those of regular pentacene [20] . To the best of our knowledge, however, no inkjet printed TIPS pentacene TFTs have been reported though there does not appear to be any barrier to doing so.

The following process was reported by *Sirringhaus et al.* to create polymer TFTs [21]. A polyimide layer is first photolithographically patterned, which uses the surface energy difference between glass and polyimide to align the source/drain layer, made of PEDOT:PSS (poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate)) , a conductive polymer. A 15-30 nm semiconductor film of F8T2 (poly(9,9-dioctylfluoreneco-bithiophene)), is spin-cast out of xylene. Next, 400-500 nm layer of PVP (polyvinylpyrrolidone), is spin cast and serves as the gate dielectric. Via holes are patterned in the dielectric by inkjet printing isopropanol, which dissolves PVP thereby creating a hole. These holes are filled with inkjetted PEDOT. As the last step, PEDOT is printed as the gate electrode.

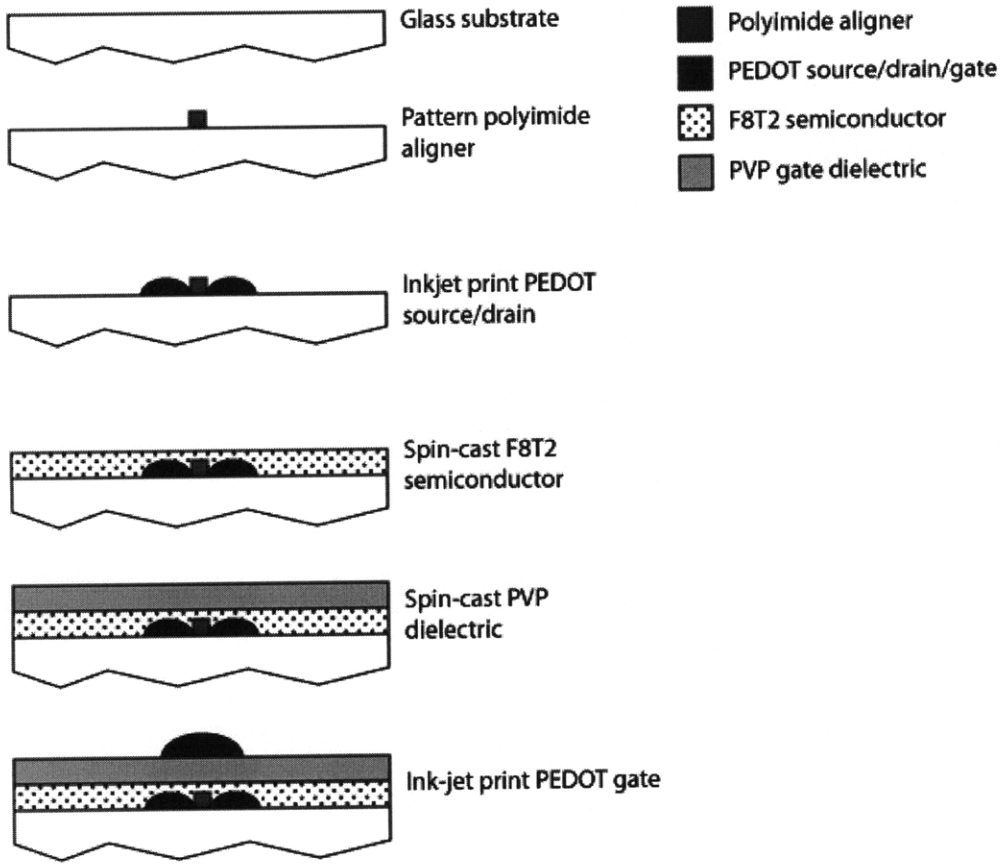

Figure 1-20: Process flow for polymer TFTs by *Sirringhaus et al.* [21].

All processing steps are done in ambient conditions, saving energy and time compared to shadow-masked and photolithographic processes which require high vacuum deposition steps. However, the mobility demonstrated for these devices is about 1-2 orders of magnitude lower than thermally evaporated small molecule thin-films. The use of polyimide necessitates curing temperatures >200°C. Lastly, there are questions regarding the stability of these devices, since PEDOT is used in place of metal contacts for the source, drain, and gate.

1.4.3 Photolithography

Photolithography is a proven patterning technique used for both silicon microelectronics and a-Si:H TFTs in the flat panel display industry. Because of its widespread use, it makes the most sense as the method to pattern organic TFTs. However, photolithographic processing of organic semiconductors is not straightforward, as solvents can adversely affect organic thin films. Therefore, processing of organic semiconductors must either avoid using harmful

solvents, or employ a method of protecting the semiconductor from solvents used in processing (such as those in photoresist).

The former approach, demonstrated by *M.Kane et al.*, uses a photosensitive aqueous solution of polyvinyl alcohol, which can be developed in water [22]. This exposure to water has been shown to not damage the pentacene film. It is, however, a non-standard resist, and can require additional heat treatments to remove water from the organic film. Pentacene can then be etched in an oxygen reactive ion etch (RIE), and the resist left on as an encapsulant.

Another approach is that first reported by *I. Kymissis et al.*, and uses an encapsulation layer to protect the pentacene film from exposure to solvent [23]. Upon evaporation of pentacene, a layer of the polymer insulator parylene-C is deposited via chemical vapor deposition (CVD). Parylene is an organic polymer insulator, deposits conformally and is relatively inert and insoluble in most solvents. This method is appealing as any type of resist can be used. Likewise, the encapsulation-semiconductor stack can be patterned by an etch in oxygen plasma.

The process pictured below is the standard OTFT photolithographic process flow used at MIT [24]. Details of this process are listed in Appendix C.

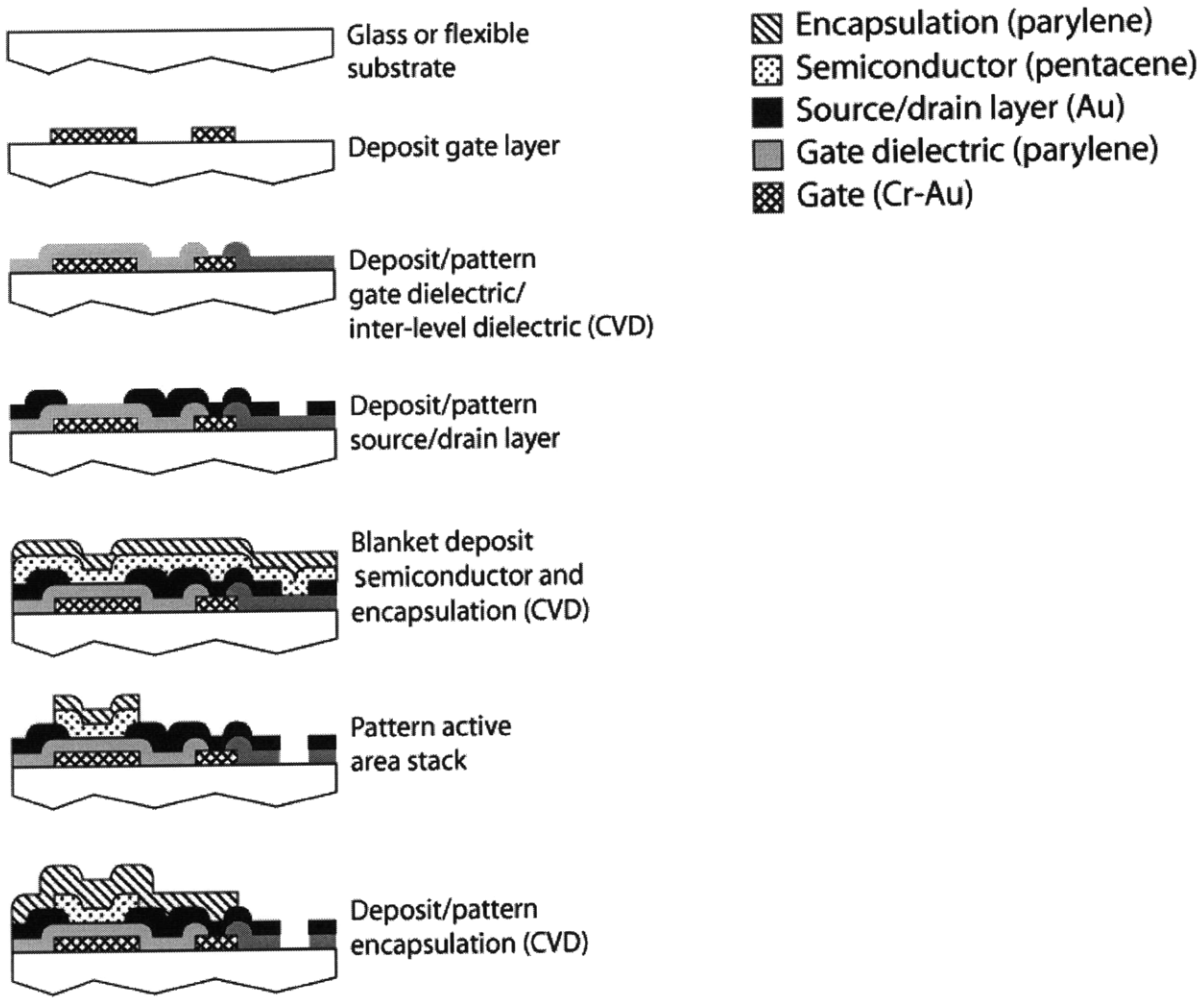

Figure 1-21: Photolithographic process flow for OTFTs.

A photolithographic process allows the use of standard CMOS processing tools, and the fabrication of micron to sub-micron channel lengths. In addition, the performance demonstrated by photolithographically processed OTFTs is comparable to that of shadow-masked devices.

One drawback, however, is the inability to pattern top contact devices. Bottom contact transistors have poorer pentacene morphology, higher contact resistance, and lower mobilities. This problem can be lessened by the use of self-assembled monolayers (SAMs) on the gold surface, which provide a more suitable surface on which the pentacene film can grow [17].

1.4.4 Photolithographic Process Layout & Device Rules

Shown below is a top-down view of a photolithographically processed OTFT.

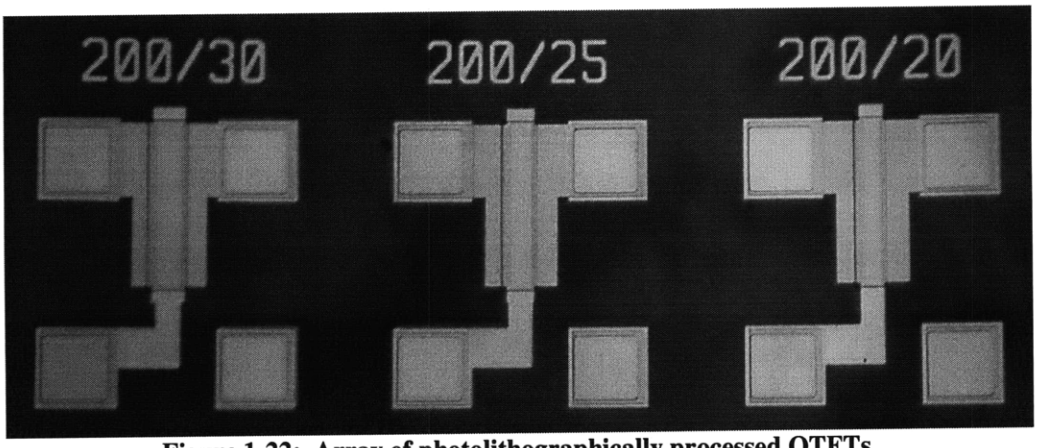

Figure 1-22: Array of photolithographically processed OTFTs.

The channel length is defined by the gap between the source and drain in the second metal layer. The standard process defines the width of the device by the width of the metal source/drain layer. This is shown below in the layout of a W=200 μm, L = 5 μm TFT.

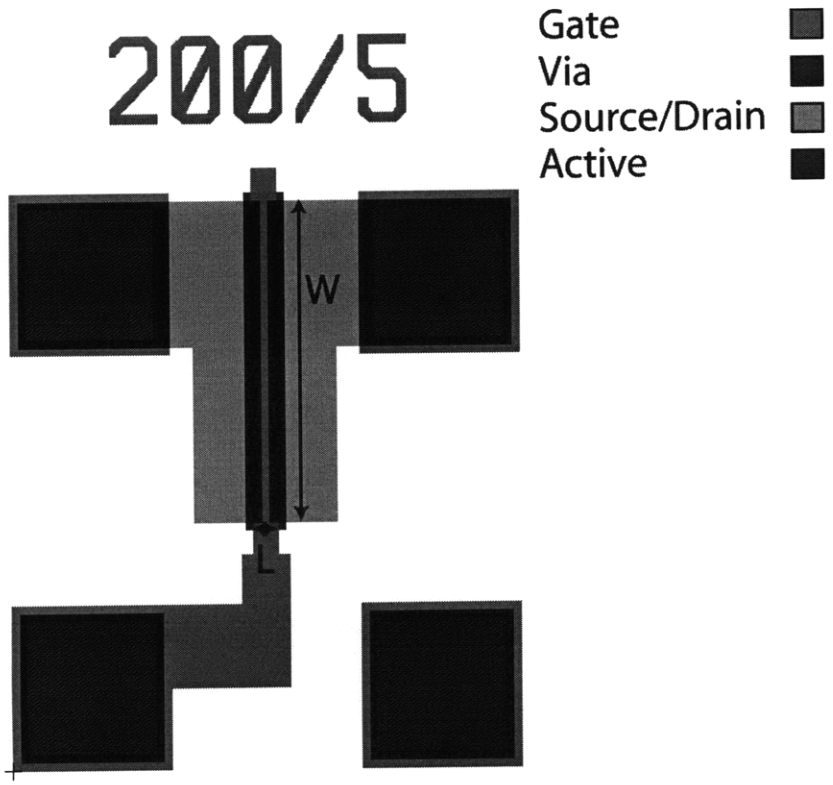

Figure 1-23: Mask layout for photolithographically patterned OTFT of W=200 μm, L=5 μm.

A number of design rules are necessary for the photolithographic process. Figure 1-24 shows a layout image, indicating each design rule. The active area extends 5 μm beyond the source drain layer (rule 1). This was done to prevent the shorting of the gate to source/drain layer by stringers [25]. The extension of pentacene beyond the source drain is gated, and contributes to the source-drain current when accumulated. Since, the pentacene extends 5 μm on each side, this extra region acts like a parasitic transistor of W= 10 μm / L= 5 μm.

This rule also extends to routing. If a source/drain trace crosses a gate layer trace, an active area pattern is drawn over the crossing point, extending 5 μm on each side. This is to prevent etching of the parylene layer and subsequent shorting of the two metal layers from stringers (rule 4).

The minimum channel length in the technology is 5 μm, which is determined by the photolithographic tools available in MTL.

Since this is not a self-aligned process, overlap between the gate and source/drain must be drawn, to ensure proper device operation in the case of misalignment. Typical misalignment of each layer is ±1-2 μm. In addition, the source/drain layer can be over-etched by as much as 1 μm. This gives a minimum tolerance of 3 μm. Therefore, 5 μm of overlap was drawn for the gate to source, and gate to drain (rule 2). The drawback of increasing the overlap is the resulting increasing in parasitic capacitance, which reduces the OTFT frequency response.

For alignment and over-etching concerns, the gate extends at least 5 μm beyond the active area (rule 3). Increasing the gate extension has no effect on device performance. It does, however, increase the device area.

Interconnects of the same metal layer must be separated by a minimum of 10 μm, to prevent shorting due to an incomplete etch (rule 6). This has no performance drawback, but again increases layout area. For routing purposes, all interconnects are at least 15 μm wide (rule 5). This is done to ensure high yield of the interconnects even in the case of poor photolithography or etching steps.

Lastly, vias are made a minimum of 10 μm x μm, and the gate and source/drain metals must extend 5 μm beyond the via (rule 7).

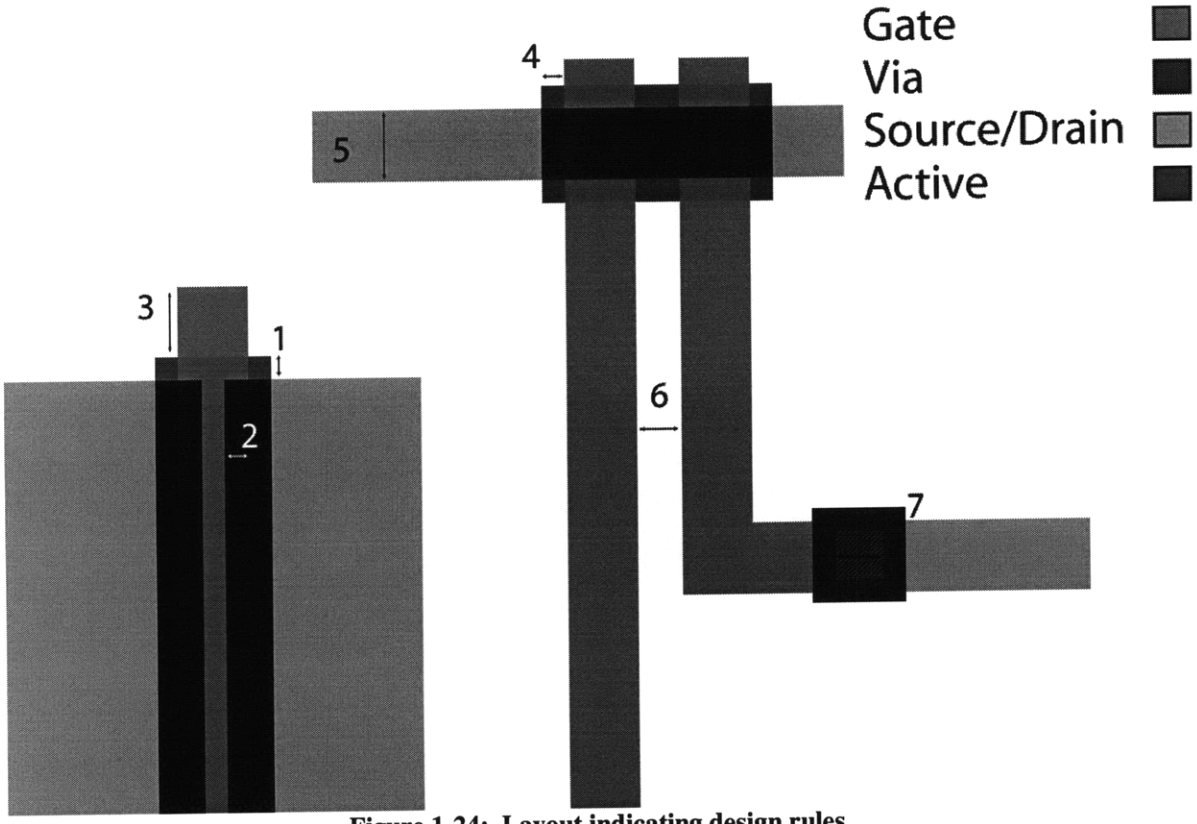

Figure 1-24: Layout indicating design rules.

Layout was drawn using L-Edit Tanner Tools software. Mask designs were exported as GDSII files, and sent to Advance Reproductions for fabrication. All masks used were 5", soda-lime glass with Cr patterns. A photograph of a completed mask is shown in Figure 1-25, along with the corresponding layout.

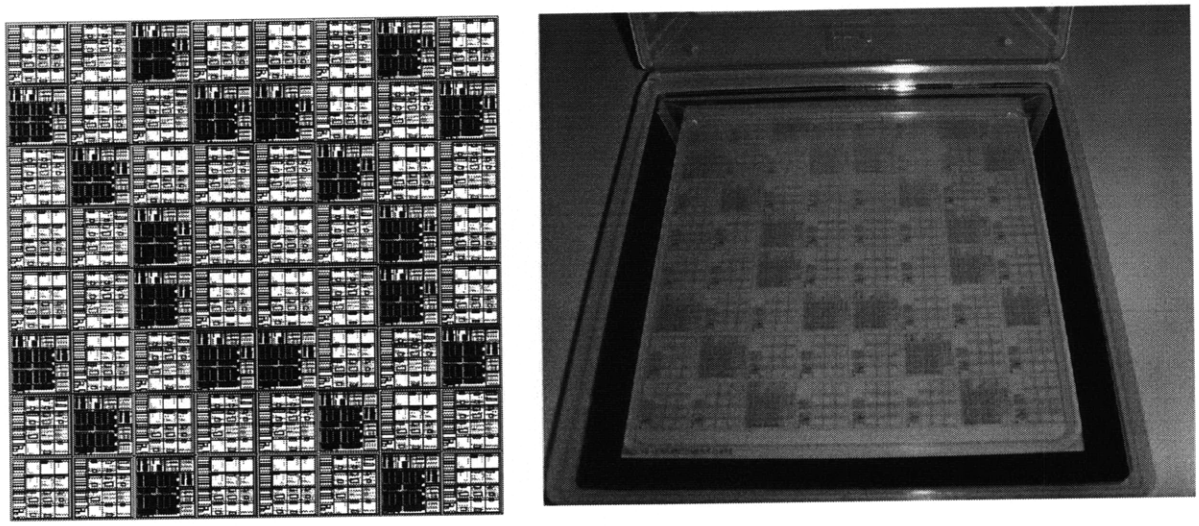

Figure 1-25: Layout and fabricated 5" soda lime/chrome mask.

1.5 Overview of Thesis

Organic semiconductors offer the potential for large-area, flexible electronics due to their near-room-temperature processing conditions. Although many individual organic transistors have been demonstrated with impressive electronic performance ($\mu \geq 1$ cm^2/Vs), few organic circuits have been reported in literature. If OTFTs are to fulfill the promise of large-area, flexible systems, OTFT technology must be developed with circuits in mind. This thesis aims to co-design OTFT devices, process technology, and circuits.

We begin by investigating the simplest application for OTFTs – an active-matrix switch. Chapter 2 adapts the conventional OTFT process to integrate an inkjet-printed organic photoconductor. Using the OTFT as a switch, an imaging pixel is demonstrated with a reponsivity of 6×10^{-5} A/V, and on/off conductance ratio of 880 at an irradiance of 5 mW/cm^2 [24]. A proof-of-concept 4x4 active-matrix imager is fabricated and tested, and demonstrated to correctly image a "T" pattern after first-order calibration.

In Chapter 3 we explore the possibility of using OTFTs as more than switching elements. Modeling of OTFTs and OTFT inverters is discussed. Simulations reveal the superiority of a zero-V_{GS} load for organic digital circuits. The area savings of a dual V_T process are discussed. A low power supply is motivated as it reduces inverter area, power consumption, and improves circuit lifetime.

A dual V_T process flow is implemented in Chapter 4. Dual threshold voltages are achieved by using high and low work function metal gates, resulting in a ΔV_T between the devices. The effect of processing conditions on device characteristics is discussed.

Chapter 5 describes digital and analog circuits using the dual V_T process. Area-minimized logic is discussed. A differential amplifier, operational amplifier and comparator using the dual V_T technology are designed and tested. These circuits use record low power supplies.

Chapter 6 discusses circuit and technology directions to improve the performance of the dual V_T circuits. The frequency response of the operational amplifier and the clocking speed of the comparator are limited due to the use of a zero-V_{GS} load. We present technology improvements to improve the speed of these OTFT circuits. A self-aligned process flow is described which uses a novel back-side exposure method to enable self-alignment. This process lowers the parasitic capacitance by almost an order of magnitude. Replacing the parylene-C gate dielectric with parylene-N and annealing prior to pentacene deposition is shown to both increase the mobility and ΔV_T. The impact of these process improvements on the circuit frequency response is discussed.

Chapter 7 summarizes the thesis' contributions, and suggests future work.

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Chapter 2 An Organic Active-Matrix Imager

A key advantage of thin-film transistors is their ability to be integrated with a number of other electronic, mechanical, or optical sensors and actuators. An active-matrix style system can be created by combining an array of sensors with thin-film transistor switches. These switches serve to connect or disconnect the sensors from row and column lines, whose voltages or currents can be read as each line is sensed, providing a 2-D map of the sensor outputs.

Use in an active-matrix system is one of the simplest applications for OTFTs. In the following chapter, OTFTs are used as switching elements for organic photoconductors, creating a 4x4 active-matrix imager. This is the first report of an organic active-matrix imager using a fully integrated process, and demonstrates the feasibility of an all organic imaging system.

2.1 Motivation and Previous Work

The ability of organic thin-film transistors to be integrated with a number of optoelectronic devices such as organic light emitting diodes (OLEDs) and organic photoconductors (OPDs) allows the creation of optoelectronic systems suitable for flexible, large area applications. Industry and academia have pursued organic semiconductor technologies for the implementation of flexible active-matrix systems such as OLED displays, and lightweight, flexible scanners [1,2].

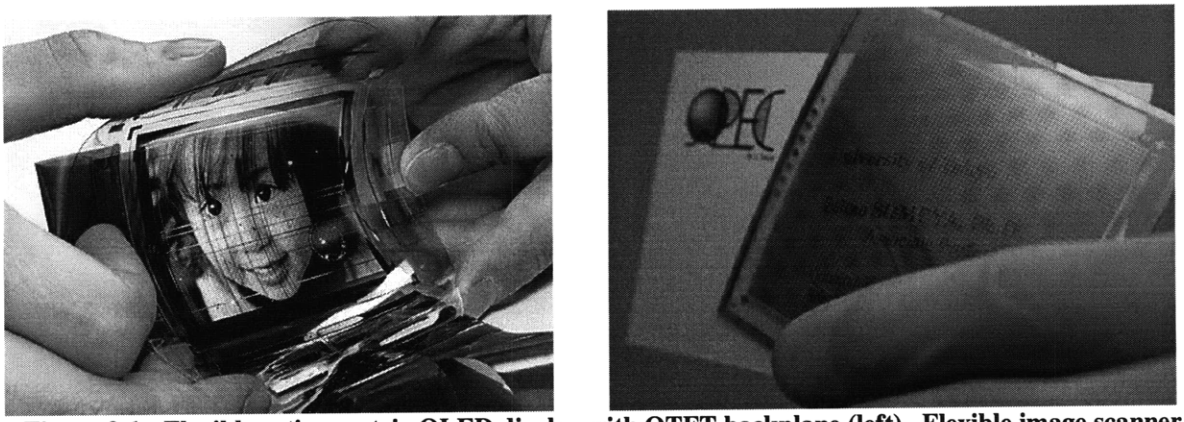

Figure 2-1: Flexible active-matrix OLED display with OTFT backplane (left). Flexible image scanner with OTFT switches and organic photodiodes (right). Source: Sony Corp., Tokyo Institute of Technology.

In particular, flexible imagers offer the potential of hemispherical electronic eyes, as suggested by *Rogers* and *Peumans* [3,4]. A prototype hemispherical silicon imager is pictured in Figure 2-2. A curved focal plane array requires less complicated lens systems and a number of other advantages over planar versions, as described by *Peumans*. In addition, large-area organic imagers would be particularly useful for x-ray medical imaging. For such an application, large area is necessary since high quality x-ray lenses are unavailable.

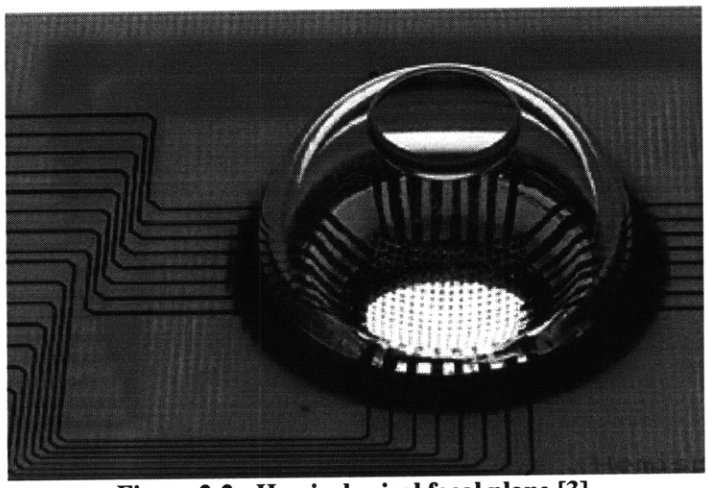

Figure 2-2: Hemispherical focal plane [3].

This is not the first report of organic-based imaging systems [2,5]. *Someya et al.* describe an active-matrix style organic imager using organic photodiodes and pentacene OTFTs, but do not fabricate all elements in an integrated process. Also, their OTFTs are fabricated via shadow-masking. *Kymissis et al.* use diode-connected OTFTs in series with organic photoconductors, and is therefore not true active matrix style. The lateral photoconductors fabricated by *Kymissis* are spincast and not patterned.

2.2 Organic TFT and Integrated Organic Photoconductor Process Flow

2.2.1 OPD Material Choice

There are thousands of organic semiconductors from which to choose a suitable photoconductor material. Several important factors when choosing the material include:

1. Absorption spectrum
2. Environmental stability
3. Compatibility with solvents

For this application, we choose titanium oxide phthalocyanine (TiOPc, $C_{32}H_{16}N_8O$ Ti). TiOPc is a common organic photoconducting material used in commercial xerographic drums, with strong absorption in green/yellow wavelengths. TiOPc, and phthalocyanines in general are known for being extremely environmentally and UV stable, and are often used as dyes in car paint and textiles. TiOPc has been demonstrated as a photosensitive material in other active-matrix systems [6].

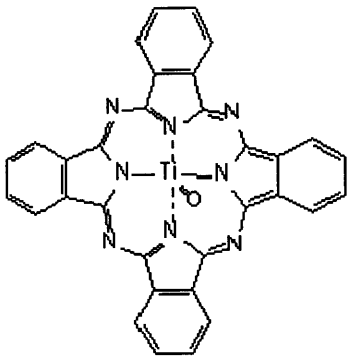

Figure 2-3: Chemical structure of titanium oxide phthalocyanine (TiOPc). Source: HW Sands Corp.

Although TiOPc is used in this instance, any air-stable organic semiconductor would likely work. By using different organic semiconductors, one could create imaging pixels sensitized to wavelengths from deep blue to red. In addition, quantum dot solutions could be used, providing even narrower absorption spectras and sensitization ranging from ultraviolet to near-infrared (NIR) [7].

2.2.2 Process Flow

This section will detail the fabrication steps for the active-matrix imager. To be suitable for large-area and flexible optoelectronics, the process flow must satisfy two constraints.

1. It must be low temperature. In order to be compatible with as many mechanically flexible, low thermal budget substrates as possible, the goal is to minimize the processing temperature.

2. It must be scalable to large areas. This requires all patterning steps to be scalable, omitting the use of shadow-mask patterning. In this process, photolithography is used to pattern all layers except the photoconductor, which is deposited via inkjet printing. Both of these processes are scalable to meters-sized substrates.

The near-room-temperature process presented successfully integrates the organic TFT with a lateral photoconductor based on a TiOPc dispersion. All processing steps except the photoconductor are done in the Technology Research Laboratory (TRL) at MIT, a class 100 cleanroom. The photoconductor is deposited in the Laboratory for Organic Optics and Electronics (LOOE). The process flow is pictured below.

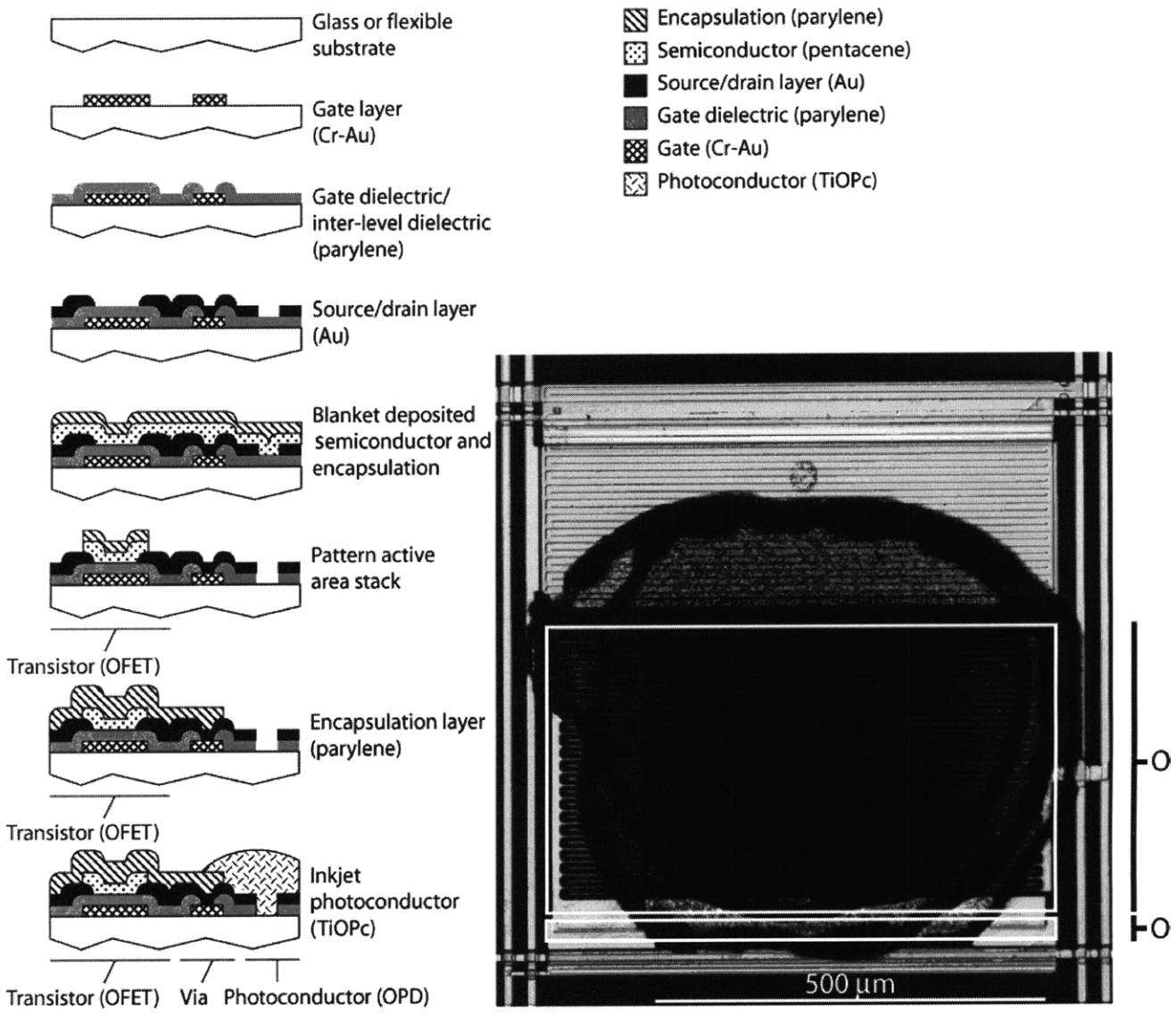

Figure 2-4: Process flow for integrated OTFT and OPD [8].

4" borosilicate glass wafers (Erie Scientific) are first piranha (1:3 H_2O_2:H_2SO_4) cleaned for 10 minutes. 10 nm of chromium and 60 nm of gold are electron-beam evaporated - the chromium layer present for adhering the gold to glass. This first layer will serve as the gate for the organic TFT and the metal 1 interconnect layer. Standard positive photoresist (OCG934) is spun at 6 seconds at 500 rpm, 6 seconds at 750 rpm, and 30 seconds at 3000 rpm. Wafers are pre-baked for 20 minutes at 95° C. Wafers are exposed for 2 seconds and are developed for 1:30. After spin rinse dry (SRD), wafers are placed in a gold etch (Transene TFA, aqueous KI/I_2), one part to 5 parts DI water, for 1:45. After SRD, wafers are immersed in CR-7 chromium etchant($(NH_4)_2Ce(NO_3)_6$ 9% by weight, $HClO_4$ 6 %, H_2O 85 %) diluted 1:1 with DI water, for 1 minute. Wafers are again SRD'd and placed into a

solvent photoresist stripper (Microstrip 2001). Wafers are agitated in microstrip for 10-15 minutes, to complete the removal of photoresist.

Next, parylene-C, an organic polymer, is deposited. It serves as the gate dielectric for the organic TFT and the inter-level dielectric between metal layers 1 & 2. Parylene is deposited by hot filament chemical vapor deposition (CVD) in a Specialty Coatings CVD system. The dielectric thickness is determined by the mass of the parylene dimer (Galaxyl) loaded. In general, there exists a linear relationship between the dimer mass and deposited film thickness, e.g. ~0.10 grams of dimer corresponds to a 100 nm thick film of parylene.

The parylene must be patterned in order to create via holes, allowing connections between metal layers 1 and 2. Image reversal photoresist (AZ5214) is spin-cast at 6 seconds at 500 rpm, 6 seconds at 750 rpm, and 30 seconds at 3000 rpm. Image reversal resist was selected as the mask layer for parylene because it was found that the negative resist profile made it easier to strip after reactive ion etch (RIE). Wafers are pre-baked for 20 minutes in 95 °C. Wafers are exposed for 1.5 seconds. This is followed by a bake for 90 seconds on a 120° C hot plate. Finally, wafers are flood exposed for 60 seconds. The wafers are then developed for 1:45, and SRD'd. The parylene is etched for 180 seconds in oxygen plasma at 100 watts in the Plasmaquest RIE tool. Again, photoresist is removed with microstrip, as detailed above.

The source/drain layer and metal 2 interconnect layer is deposited next. 40 nm of gold are electron-beam evaporated. We have found that depositing the gold via electron-beam evaporation results in less hysteretic devices than those in which the gold is deposited by sputtering. We suggest that the parylene could be damaged by the argon plasma during sputter deposition. The OCG positive photolithography process is the same as described above. The gold is patterned by immersing the wafers for 1.5 minutes in Transene TFA gold etchant, diluted 5 parts DI water to 1 part etchant. The photoresist is removed in microstrip.

Wafers are then moved to the pentacene evaporator for deposition of the TFT channel material. Upon reaching a base pressure of at most 10^{-6} torr, pentacene is thermally evaporated by heating the crucible to approximately 210° C. 10-15 nm of pentacene is evaporated at a typical rate of 0.5-1 nm/minute.

We are able to photolithographically pattern pentacene by a process first introduced by I.Kymissis, described in Chapter 1. To prevent the pentacene from solvent damage, a 150 nm encapsulating layer of parylene-C is deposited. OCG photoresist is spin cast on the pentacene/parylene stack, and etched at 100 W for 180 s in oxygen plasma.

The active area of each transistor is now defined, and the transistor is completed. We note that transistors characterized after this step, and those characterized after completion of the photoconductor display a number of differences. This will be discussed later in this section.

Another layer of parylene serves to encapsulate the transistors, and isolate the TFTs from the photoconductor. In addition, this step creates a "well" for the TiOPc dispersion to reside,

aiding in patterning and preventing the material from spreading beyond the pixel. 150 nm of parylene is deposited via CVD, and is patterned with OCG resist and RIE. After the photoresist is stripped, the exposed gold interdigitated fingers are ready for deposition of the photosensitive material.

A proprietary Hewlett-Packard thermal inkjet printing system (TIPS) is used to additively pattern the photoconductor material. The experimental set-up of the printing tool is shown below, built by the author and I. Kymissis.

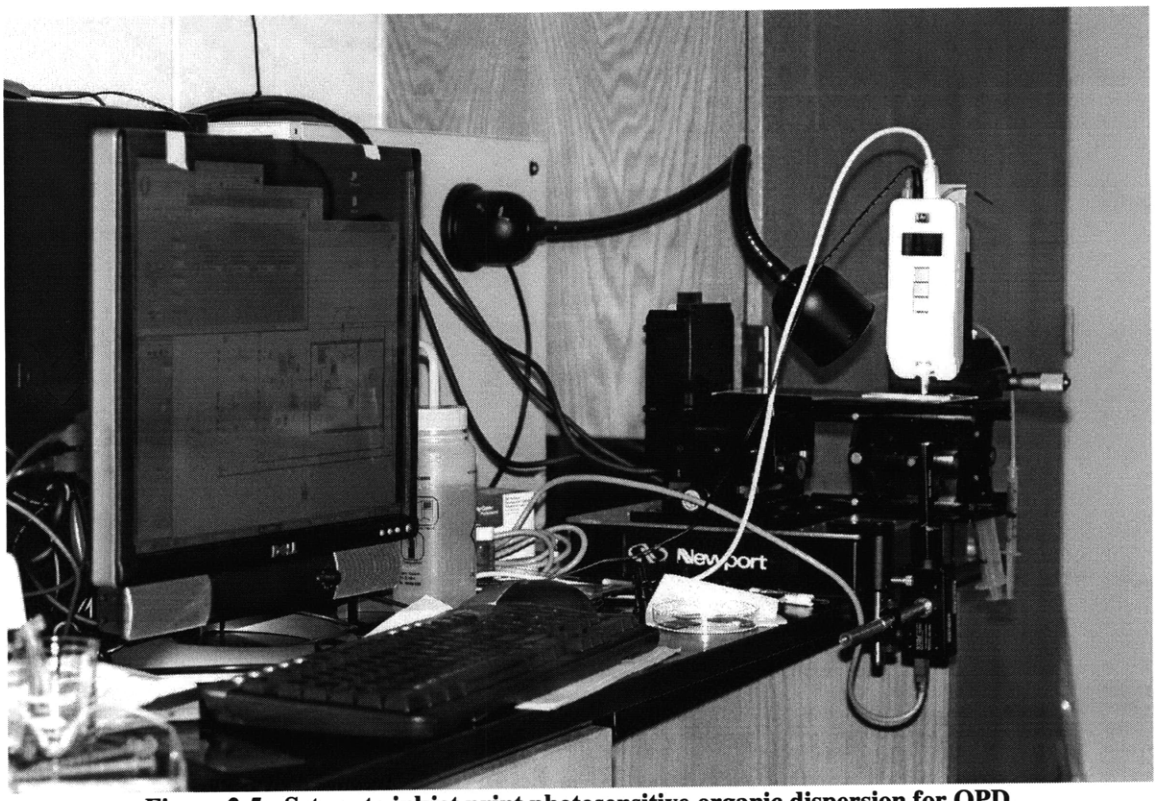

Figure 2-5: Set-up to inkjet print photosensitive organic dispersion for OPD.

The printing tool is mounted vertically to an x-y stage. A glass pane is situated below the printhead and mechanically supports the wafer while maintaining transparency. This is necessary for alignment, as an electronic camera sits below the glass substrate and displays an image of the wafer to the computer, allowing the user to align the printhead to the wafer. The inkjet tool is software controlled.

A colloidal dispersion of gamma phase TiOPc (4.2% by weight) in ethyl acetate & butyl acetate (1:1) (94% by weight) and polyvinylbutyral (1.8% by weight), purchased from H.W. Sands, was further diluted in butyl acetate (70:1). This dispersion was filtered with a 5 micron filter (Millipore), and then loaded into a 220 pL inkjet print head. The filtration was necessary to prevent large particles in the dispersion from clogging the microelectromechanical system (MEMS) print head.

The dispersion concentration, number of drops on each photoconductor pixel, and drying time between drops were all optimized for maximum photoresponse. The settings were as follows: continuous burst, 800 ns prepulse, 1 μs gap, 2100 ns pulse width, 29.25 V, and 100 drops per pixel. An optical micrograph from a completed wafer shows the OFET and OPD and is pictured with the process flow in Figure 2-4.

2.3 Device Characterization

2.3.1 Organic TFT

OTFTs and OPDs were fabricated, and electronically and optically characterized. Current-voltage, and capacitance-voltage characteristics for the OTFTs were measured using an HP 4156C semiconductor parameter analyzer. Device parameters such as the mobility and contact resistance were extracted in the same manner as described in Chapter 1.

Changes in the electronic performance of the OTFTs before and after photoconductor processing were observed. Semilog transfer characteristics in saturation (V_{SD}=20 V) for 1000 μm/25 μm devices before and after processing are pictured in Figure 2-6.

By applying a linear fit to the semilog transfer curve in the subthreshold region and noting at which voltage this linear fit deviates from the I-V, we are able to obtain the threshold voltage. The fresh OTFT pictured on the left has a threshold voltage of -1 V. After photoconductor processing, the device has become more depletion-mode and has a threshold voltage of 4 V. The subthreshold slope is also seen to degrade from approximately 500 mV/decade to ~1 V/decade.

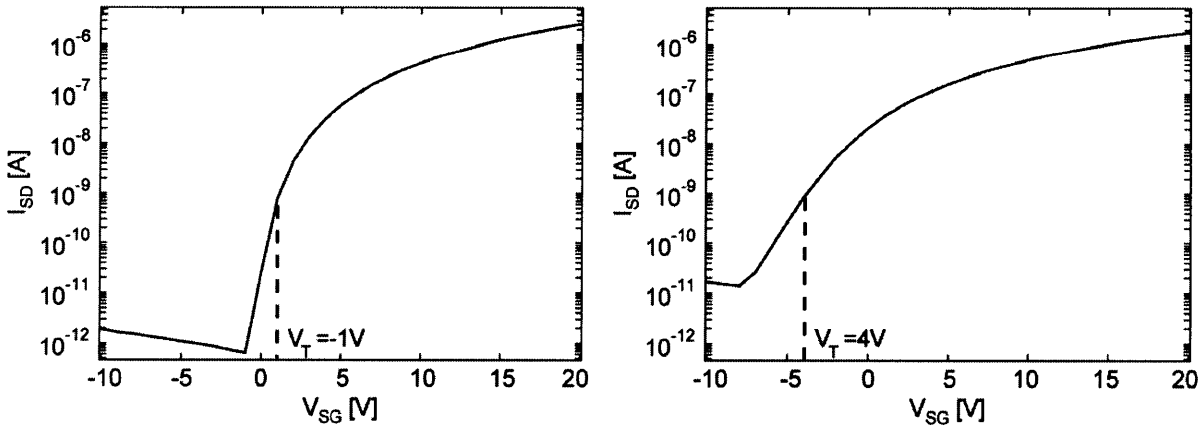

Figure 2-6: Measured transfer curves of W=1000 μm, L=25 μm device, V_{SD}=20 V. Device on left is measured immediately after OTFT fabrication. Device on right measured after OPD processing.

Two possible reasons for this observation are suggested. It has been reported that oxygen plasma exposure of parylene prior to deposition of pentacene results in a shifting of the threshold voltage more positive, and an increase in the subthreshold slope [9]. The exposure of the OTFTs to oxygen plasma during photoconductor processing may be source of these effects.

Also, solvent exposure during photoconductor processing may affect the OTFTs. Reports in literature indicate that solvents can induce phase transformations in pentacene, affecting the microstructure and current-voltage characteristics of the OTFT [10].

By using the method of *Ryu et al.* to extract mobility, we can confirm that the device after photoconductor processing exhibits lower carrier mobility [11]. The mobility versus overdrive voltage ($V_{SG}+V_T$) is plotted for both devices pictured in Figure 2-7. It is also important to note that the overdrive voltage of the post-OPD processed device is higher, due to its more positive V_T.

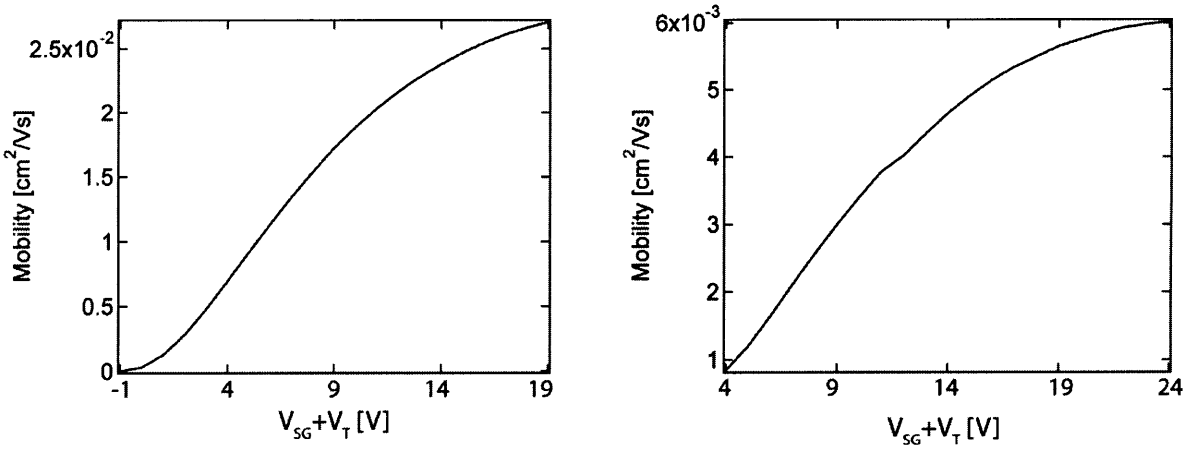

Figure 2-7: Measured mobility of OTFT immediately after OTFT processing on left. Mobility of OTFT after OPD processing on right. V_T of device on left =-1 V, V_T of device on right=4 V. Same devices pictured in Figure 2-6.

2.3.2 Organic Photoconductor

The OPD's optical response was characterized by illuminating it with a specified wavelength and measuring the current through the device. After calibrating the light source with a silicon photodetector, the percentage of photons absorbed by the OPD can be obtained. Lastly, by sweeping the illumination wavelength, the percentage of absorbed photons and measured current can be plotted as a function of wavelength.

Doing these measurements allows one to obtain the external quantum efficiency (EQE) of the OPD. The experimental setup is pictured in Figure 2-8.

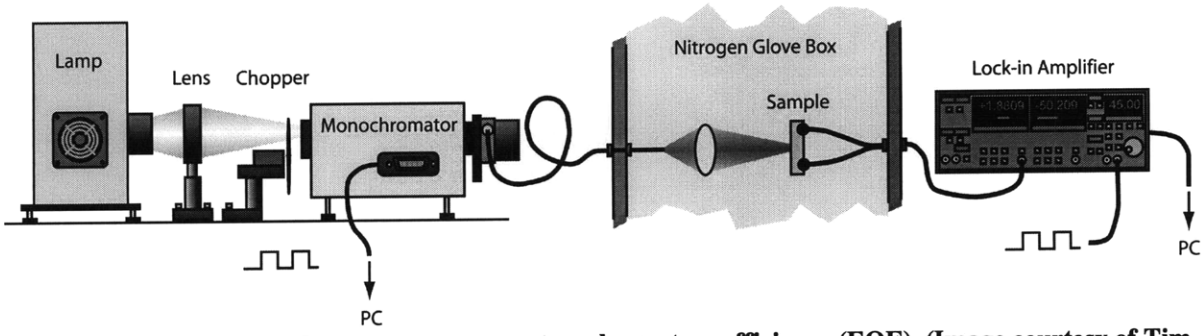

Figure 2-8: Experimental setup to measure external quantum efficiency (EQE). (Image courtesy of Tim Osedach)

The photoconductor was illuminated by a Xe lamp filtered by a monochromator, chopped at 95 Hz and referenced to a Newport 818 UV calibrated photoconductor. A SR 830 lock-in amplifier sensed the photoconductor current as the illumination wavelength was varied. The external quantum efficiency versus wavelength is plotted below.

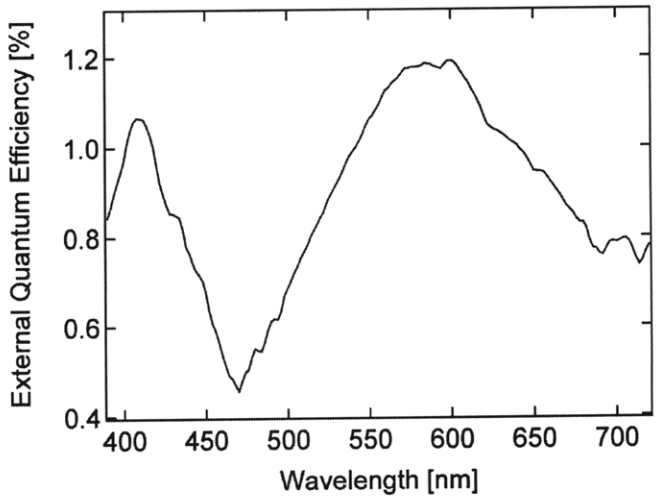

Figure 2-9: Measured external quantum efficiency for OPD.

The EQE is highest around 600 nm, similar to what has been reported for the photoluminescence spectrum of TiOPc [12]. To understand how we arrive at this number, we can describe the EQE as a product of multiple efficiencies.

$$\eta_{EQE} = \eta_{absorption} * \eta_{excitondissociation} * \eta_{carrierextraction} \quad (2\text{-}1)$$

To improve the EQE, these individual efficiencies must be increased. Since the photoconductor is almost transparent to the eye, it is obvious that most of the incident light is not being absorbed. By increasing the thickness of the OPD layer, more light will be

absorbed, thereby increasing the absorption efficiency. If all the incident light is absorbed, $\eta_{absorption}$ becomes 100%.

When the photon is absorbed, it creates a bound electron-hole pair known as an exciton. Since excitons have no net charge, they must be dissociated before they can be drifted by the applied electric field and measured as current at the contacts. Each organic semiconductor has a characteristic exciton diffusion length – that is, the average length an exciton can diffuse before it recombines. To improve EQE, we must minimize exciton recombination. Dissociation will take place at an interface, therefore we can improve the exciton dissociation efficiency by decreasing the size of the TiOPc crystals. Or, a material with a longer exciton diffusion length could be used in place of TiOPc.

Lastly, once the excitons are split into electrons and holes, these individual carriers must be extracted before they themselves recombine. The carrier extraction efficiency can be improved by increasing the field across the OPD. A higher field will decrease the transit time of the carriers, decreasing the chance of recombination in the OPD. Although a higher field could be obtained by increasing V_{DD}, we also wish to decrease the power supply of the entire system. Therefore, decreasing the gap between electrodes would increase the field and extraction efficiency while leaving the power supply constant (or even lowered).

2.4 Pixel Circuit

By connecting the OTFT and OPD in series, we can create a simple pixel circuit. When a V_{SG} of 20 V is applied, the OTFT is in accumulation and serves as a low resistance switch in series with the OPD. In this configuration, the current through the pixel is determined by the OPD resistance, which is a function of the incident luminance. When the OTFT is in cutoff (V_{SG}=-5 V), there are no accumulated holes in the OTFT, and the pixel resistance is dominated by the OTFT. Therefore, the pixel current is not dependent on the incident light intensity. In order for the ratio of the OPD and OTFT resistances to be correct during both modes of operation, one must carefully design the width and length of both devices.

The schematic of the pixel is shown below. A width 1000 μm and length 5 μm OTFT is used as the switch. The OTFT has an "on" conductance of 20 nS, and an "off" conductance in the 100s of fS. Because of the depletion-mode behavior of the OTFT, the "off" state requires a V_{SG} of -5 V. The "on" state corresponds to a V_{SG} of 20 V. The lateral photoconductor is sized with an effective width of 25 mm, and an electrode gap spacing of 5 μm.

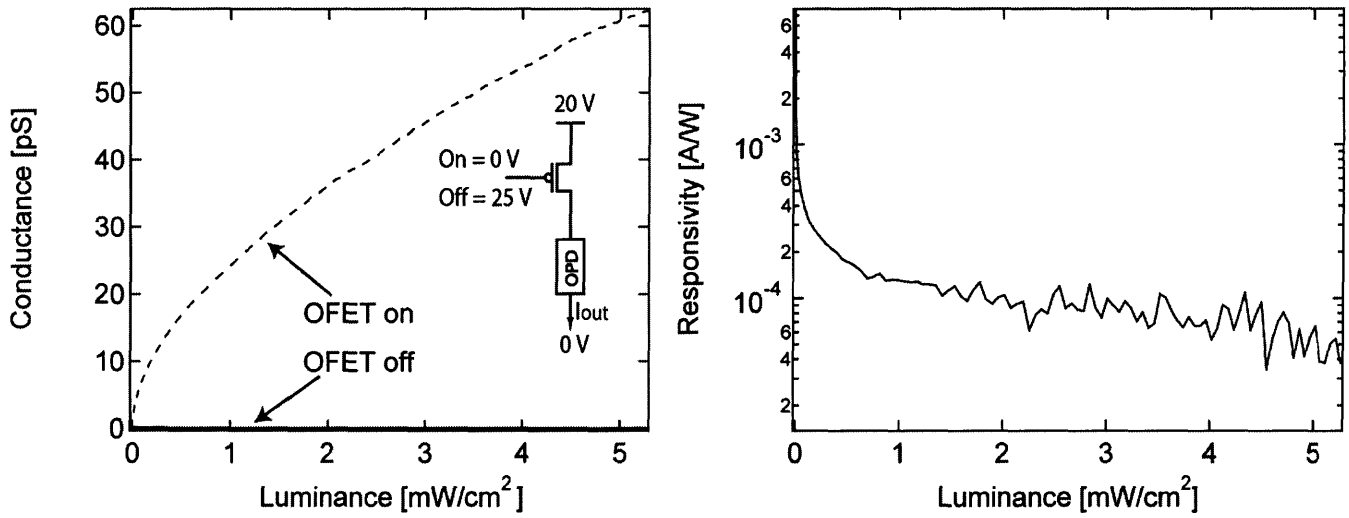

Figure 2-10: Measured conductance as a function of illumination luminance (left). Pixel responsivity as a function of luminance (right).

For comparison, direct sunlight corresponds to an irradiance of 10 mW/cm^2 . At an illumination of 5 mW/cm^2 , the pixel exhibits a conductance on/off ratio of 880, and a responsivity of $6x10^{-5}$ A/W. The responsivity was calculated using the following equation, where V is the applied voltage, and G the pixel conductance.

$$Responsivity = \frac{V * G}{Irradiance * Area} \qquad (2\text{-}2)$$

The responsivity was calculated by assuming the entire pixel area was collecting light, which we shall see later is an overestimate. Therefore the actual responsivity is slightly higher than what is plotted in Figure 2-10.

The organic transistor is sized such that it is at least an order of magnitude more conductive than the OPD when on, and greater than 10 times more resistive than the OPD when off. This ensures a window of correct operation of the pixel, even if the OTFT degrades over time.

2.5 Active-Matrix Imager

A 4x4 proof-of-concept imaging array was designed using the pixel element above. The circuit schematic of the imager is shown below.

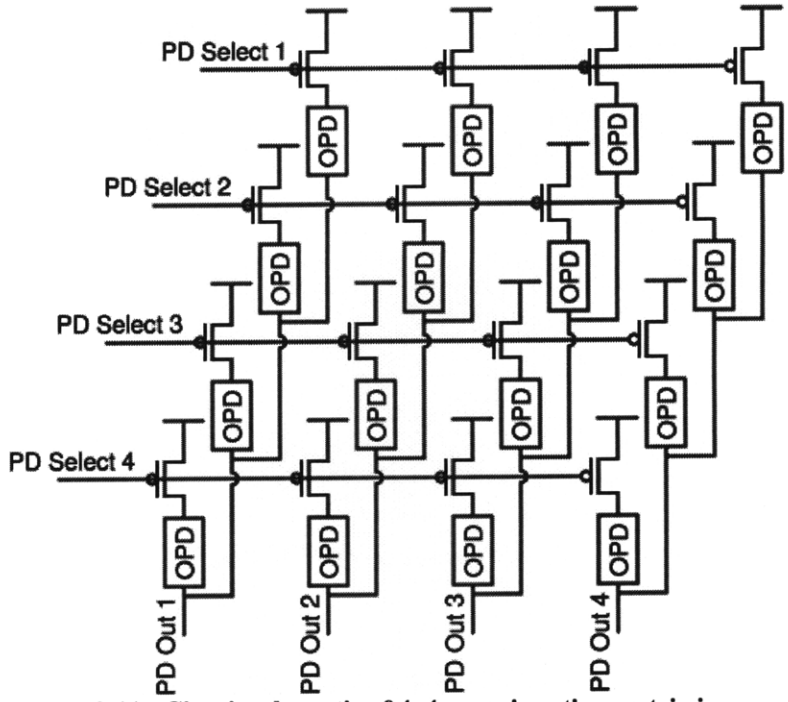

Figure 2-11: Circuit schematic of 4x4 organic active-matrix imager.

In this circuit, we turn PD Select 1 high (0 V), and the current at PD Out 1 is sensed with the 4156. The PD Select 2-4 and PD Out 2-4 lines are rastered through until all pixels are accessed.

A die photograph of the fabricated imager is shown below. It occupies an area of 10.24 mm^2. From this image, there are two important notes: one, the photosensitive area does not cover the entire OPD area, and two, there is a notable variation in OPD area between pixels.

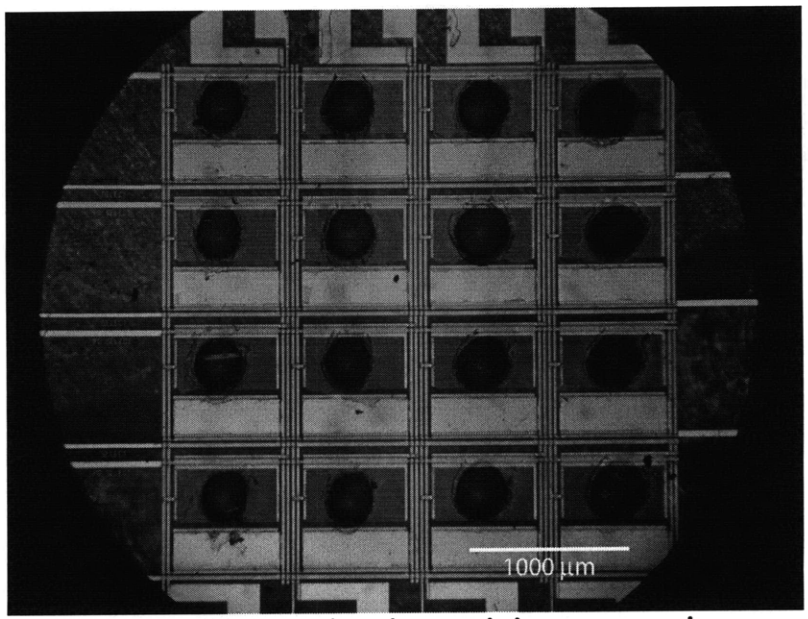

Figure 2-12: Die photograph of 4x4 organic active-matrix imager, occupying an area of 10.24 mm^2.

The variance in photosensitive area can also be seen if one measures each pixel conductance upon illumination by a uniform light source. This is pictured below.

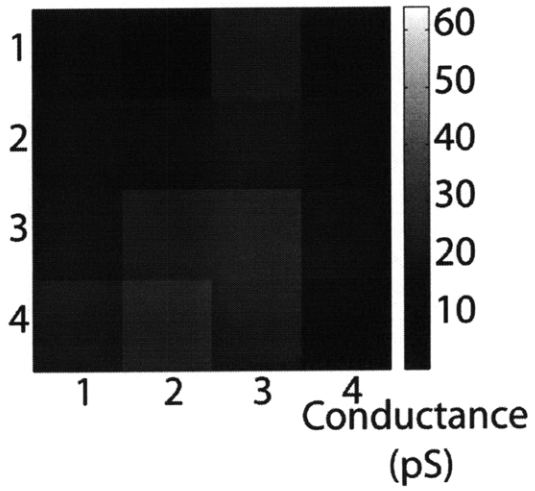

Figure 2-13: Map of pixel conductances under uniform illumination, showing fixed pattern noise.

Because of this fixed pattern noise, we must do a calibration in order to correctly image a pattern. The first-order calibration is done as follows.

1. The pixel conductances under a uniform, measured intensity are recorded (Figure 2-13).

2. Next, the test image is placed on the imager. In this case, a "T" shadow obscures light from a 530 nm Lumileds LED. This is pictured below. Under the test pattern, each pixel conductance is recorded. It is important to note that the right part of the "T" only partially obscures the photosensitive area of those pixels, as can be seen in Figure 2-14.

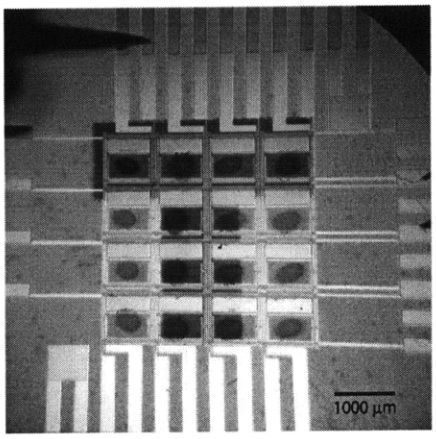

Figure 2-14: Imager under 530 nm illumination and test "T" pattern.

3. To obtain the correct pixel brightness under the test image, the following linear equation is used.

$$\frac{G_{pattern}}{G_{calibration}} * L_{calibration} = L_{pattern} \tag{2-3}$$

Calculating the luminances for each pixel results yields Figure 2-15.

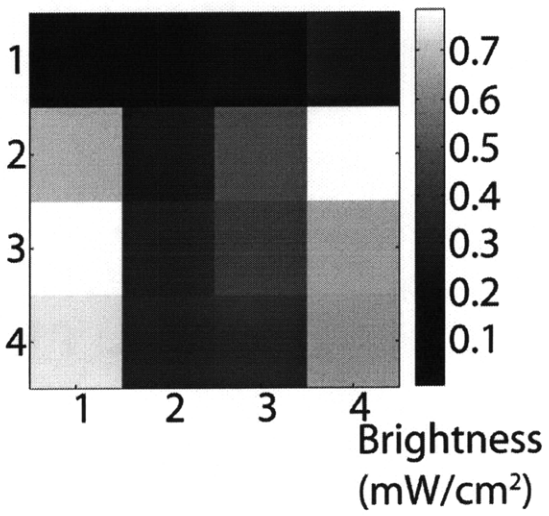

Figure 2-15: Imager brightness under "T" pattern, after first order calibration.

Figure 2-15 indicates the "T" pattern is clearly visible, and that the right part of the "T" is brighter, which makes sense given that the shadow only partially covers those OPDs.

2.6 Summary

An integrated process flow for pentacene OTFTs and TiOPc OPDs was presented. During fabrication, the substrate sees a maximum temperature of 95°C, ensuring its compatibility with mechanically flexible plastic substrates. OTFTs' current-voltage characteristics were shown to change before and after OPD processing, possibly due to exposure to oxygen plasma and solvents. The OPD was measured to have a maximum EQE of 1.1% at approximately 600 nm.

A pixel circuit consisting of an OTFT in series with an OPD, and was measured to have a conductance on/off ratio of 880 and a responsivity of 6×10^{-5} at a luminance of 5 mW/cm^2. A

4x4 active matrix imager was fabricated and tested. Fixed pattern noise could be reduced by performing a first-order calibration. After the calibration, a "T" pattern was successfully imaged.

Future work should aim to improve the external quantum efficiency of the OPD to reduce the minimum pixel size and increase imager resolution.

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Chapter 3 Trade-offs in Circuit Design with OTFTs

Although individual OTFTs have been demonstrated with impressive performance, namely high carrier mobilities, circuit design in organics is a nascent field. There have been very few reports of positive noise margin inverters and rail-to-rail ring oscillators. There is only one report of analog circuits such as operational amplifiers.

Designing circuits in organic technologies is difficult because of four reasons:

1. Absence of a complementary load
2. Only a single V_T, p-channel device available
3. The value of the V_T
4. No resistors

In this chapter, a framework for inverter design with OTFTs in a conventional organic PMOS-only technology is described. Through modeling and simulations, we describe the impact of parameters such as the V_T, V_{DD}, and circuit topology on noise margins. The benefits of a two threshold voltage process are described. Lastly, lowering V_{DD} is shown to reduce the area requirements in OTFT circuits, and improve circuit lifetime due to reduction in the bias-stress effect. Although other work has studied the effects of device parameters and V_{DD} on OTFT inverters assuming a long-channel Si model, to the best of our knowledge this is the first quantitative investigation of trade-offs in OTFT inverters using models based on measured data [1].

3.1 Modeling OTFTs

Design trade-offs in OTFT circuits were investigated through simulation. In order to simulate circuits, however, one must first model the individual devices. Previous work in the group adapted the RPI amorphous silicon model for OTFTs [2,3]. Details of the model are described in Appendix A and a thorough derivation is given in [2].

Figure 3-1 compares the output curves generated by the model with measured results for a W=200 μm, L=25 μm device. We see there is excellent agreement between the model and

measured output curves. Further verification of the model versus measured OTFTs is shown in [2].

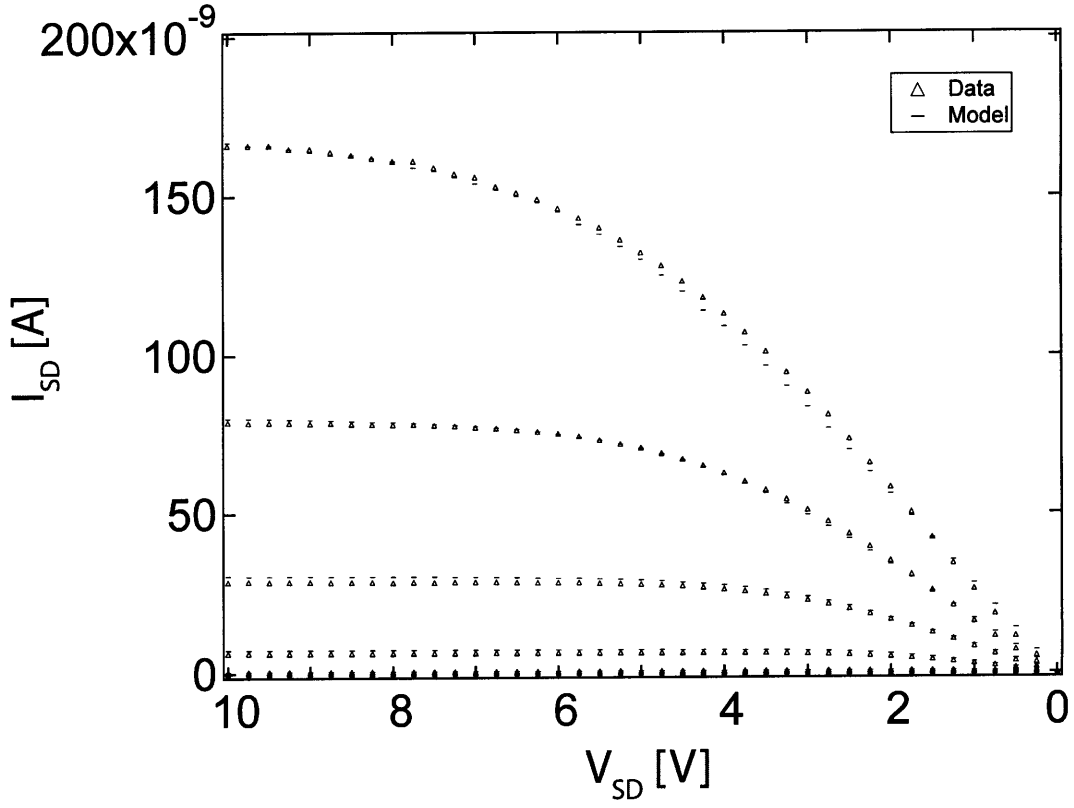


Figure 3-1: Measured and simulated output curves for W= 200 μm, L= 25 μm device. V_{SG} stepped from -0 V to 10 V, in 2 V increments.

Now that the current-voltage characteristics of a device can be modeled, a simple circuit simulator can be implemented by instantiating this model for all devices in the circuit. The following section describes the simulation of OTFT inverters. In particular, we are interested in the trade-offs between the inverter topology, device geometry, threshold voltage, power supply, and the large signal characteristics of the circuit. The next section discusses these trade-offs.

3.2 Modeling OTFT Inverters

3.2.1 Diode-load Inverter

The inverter is the most basic digital circuit, and the fundamental building block for larger digital systems. If OTFTs are to be used for any integrated systems beyond active-matrix switches, inverters will be necessary, whether as a part of control logic, static random access memory (SRAM), or larger digital circuits. Therefore, a working OTFT inverter must be demonstrated as the first step towards organic integrated circuits. In OTFT literature, only a few instances of operational inverters have been reported.

An ideal inverter, connected to a power supply V_{DD} and ground, is shown below. The purpose of an inverter is to output a voltage which is the complement of the voltage input. When the input to the inverter is low (less than $V_{DD}/2$) it outputs a high voltage, V_{DD} (i.e. a "1"). When the input is high (greater than $V_{DD}/2$) the inverter outputs a low voltage, 0 V (i.e. a "0"). If the input is exactly at $V_{DD}/2$, the inverter is in a metastable state. Since an ideal inverter has infinite gain, any small deviation in input voltage will cause the output to swing to V_{DD} or ground.

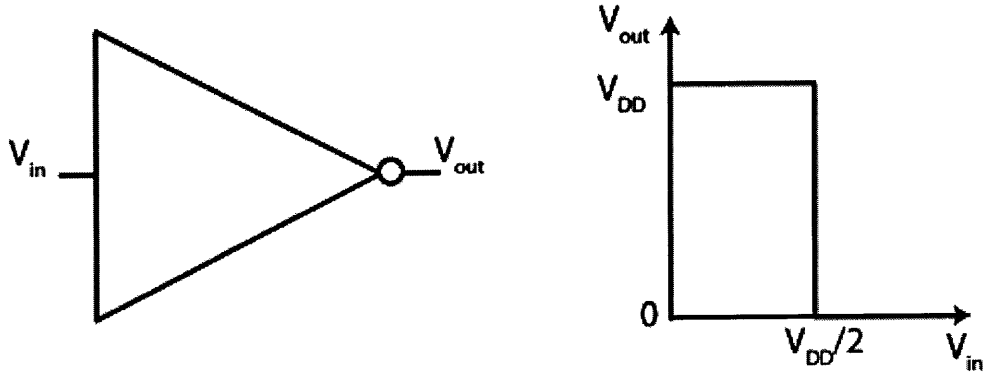


Figure 3-2: Ideal inverter transfer characteristics.

The inverter is implemented by a simple voltage amplifier, with gain $-A_V$. This circuit typically contains two transistors, the driver – whose gate takes the inverter input, and the load, which provides high output resistance. In OTFT technology, resistors are typically unavailable, therefore an active device must be used as the load.

By successfully modeling the OTFT current-voltage characteristics, one can determine the DC characteristics of an OTFT circuit consisting of an OTFT driver and load. The DC inverter characteristics are found by performing load-line analysis, and finding the circuit's output voltage for each input voltage. This function was implemented in a MATLAB script. This is included in Appendix B.

As an example of the method and simulator, we show the following OTFT inverter which consists of a driver device and OTFT load. The load's gate is connected to its drain. Therefore, $V_{SG}=V_{SD}$, and the device's output curve looks like a diode - this is why a load with its gate and drain shorted is called "diode connected". Its small signal output resistance is $\sim 1/g_m$.

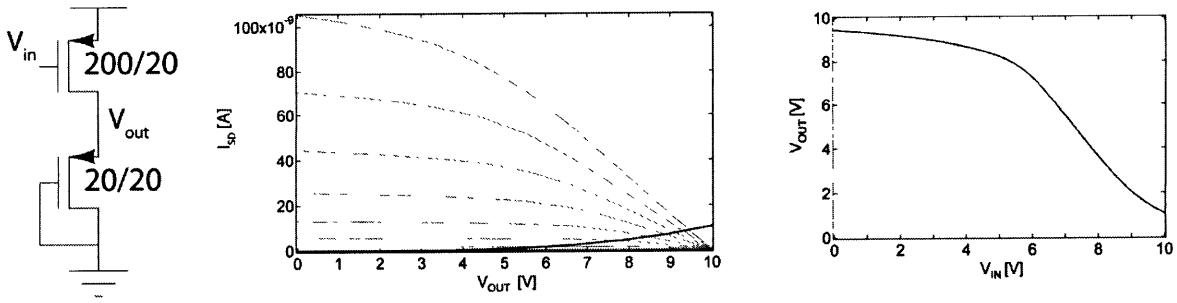


Figure 3-3: Diode-loaded inverter, load line analysis, inverter output curve extracted from load line analysis, V_{DD}=10 V.

Once the device sizes and circuit topology are input, one can generate the output curves and perform the load line analysis. At each V_{IN} value, the script finds V_{OUT}, i.e. the intersection point between the two curves. The script finds the intersection by taking the difference between the two curves, and finding the minimum of the difference. This analysis generates the inverter DC transfer characteristics. Figure 3-3 shows an example of this process with a diode-loaded inverter.

Now that we have the inverter transfer function, one can quantify the performance of the inverter. The most important metric we use is the noise margin, which describes the robustness of the inverter to spurious signals at its input. The noise margin is the largest deviation from a "high" or "low" voltage the circuit can tolerate at its input and still output the correct logic level. The noise margins must be positive for an inverter to work properly. The more positive the noise margins, the better.

The noise margin high (NM_H) and noise margin low (NM_L) are defined by the following equations [4].

$$\begin{aligned} NM_H &= V_{OH} - V_{IH} \\ NM_L &= V_{IL} - V_{OL} \end{aligned} \tag{3-1}$$

The output voltage high (V_{OH}), input voltage high (V_{IH}), output voltage low (V_{OL}), and input voltage low (V_{IL}) are found at the points where the inverter transfer function reaches a gain of -1 V/V. For the ideal inverter shown in Figure 3-2, NM_H=V_{DD}/2, NM_L=V_{DD}/2. The sum of the noise margins can be no greater than the power supply, V_{DD}.

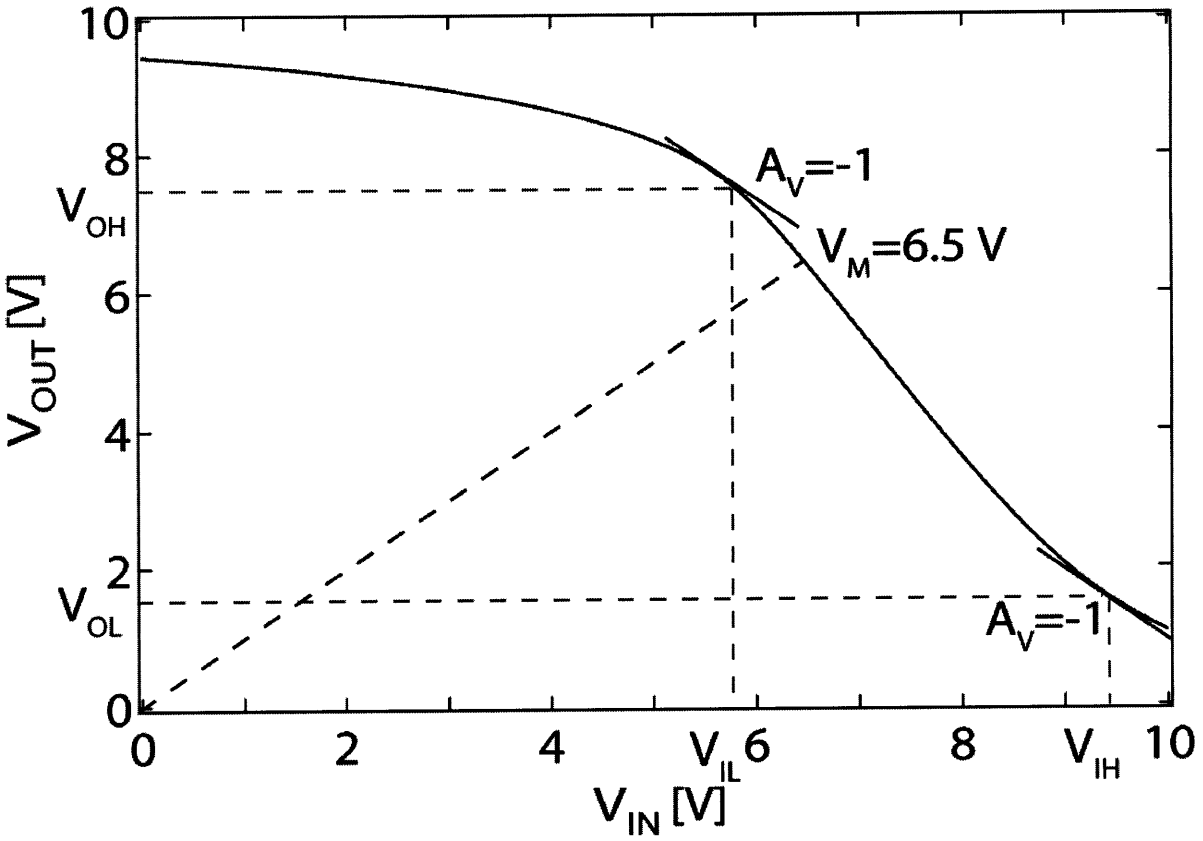


Figure 3-4: Output curve for inverter in Figure 3-3, indicating voltages where gain=-1. V_M = 6.5 V.

The V_{OH}, V_{OL}, V_{IH}, V_{IL} are illustrated above for the diode-loaded inverter of Figure 3-3. For this inverter, the NM_H=-1.6 V, NM_L=4 V. In other words, this circuit does not properly behave like an inverter. The negative noise margins are due to the low gain of the diode-load inverter and the asymmetry of the trip voltage (V_M). The voltage gain for this topology at V_M is shown in Equation 3-3.

$$A_v = -g_{m,driver} x \left(\frac{1}{g_{m,load}} \| r_{o,driver} \right) \Big|_{V_M} \approx -\frac{g_{m,driver}}{g_{m,load}} \Big|_{V_M} \tag{3-3}$$

Using our result for g_m from Chapter 1, Equation 3-3 can be re-written. Inserting the transconductance equation found in Chapter 1, one finds that the gain of the diode load can be expressed by Equation 3-4.

$$A_v = -\frac{g_{m,driver}}{g_{m,load}} = -\frac{\left(\frac{1}{\mu}\frac{d\mu}{dV_{SG}}\sqrt{I_{SD}} + \sqrt{2\left(W/L\right)_{driver} C_{ox}\mu}\right)}{\left(\frac{1}{\mu}\frac{d\mu}{dV_{SG}}\sqrt{I_{SD}} + \sqrt{2\left(W/L\right)_{load} C_{ox}\mu}\right)} \tag{3-4}$$

If we neglect the change in mobility with respect to V_{SG}, one finds that the gain is only dependent on the square root of the ratio of the W/L's of the devices. This is the classic relationship for diode-load inverters in silicon MOS. If we consider the effect $d\mu/dV_{SG}$, one sees that the increase in mobility with respect to V_{SG} lowers the gain of the diode-load inverter. The mobility dependence on V_{SG} "dilutes" the effect of the W/L difference between the driver and load. If $d\mu/dV_{SG}$ is large, the gain trends towards -1. Ideally, one would want $d\mu/dV_{SG} = 0$ to maximize the gain.

One would imagine making the ratio of sizes even larger to realize a higher gain. Doing so makes V_M move even closer to V_{DD} causing V_{IH} to move more positive, reducing noise margins.

3.2.2 The Effect of V_T on Noise Margins

The simulator allows one to sweep through values of V_T and obtain the noise margins for a given inverter topology. These simulations will indicate how sensitive OTFT diode-loaded inverters are to V_T, and if there is any range of V_T's that yield positive noise margins.

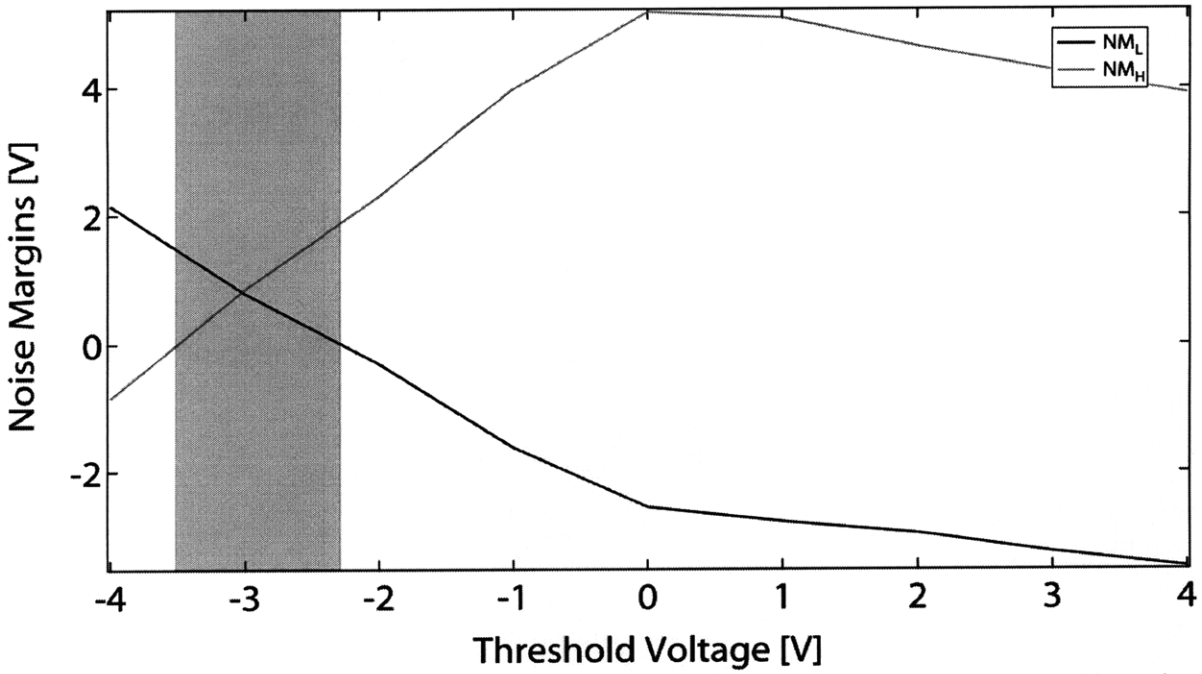


Figure 3-5: Noise margins for diode loaded inverter, V_{DD}=10 V, device ratio=10:1. Area of positive noise margins indicated by blue rectangle.

The plot above indicates that a 10:1 sized diode-load inverter will only give positive noise margins for a V_T= -2.9 ±0.6 V. The performance is little improved if we move to a 100:1 sized diode load inverter. In this case, positive noise margins can only be obtained with a V_T= -2.9 ±0.9 V. Using a 1000:1 sized diode load inverter worsens characteristics and is not shown.

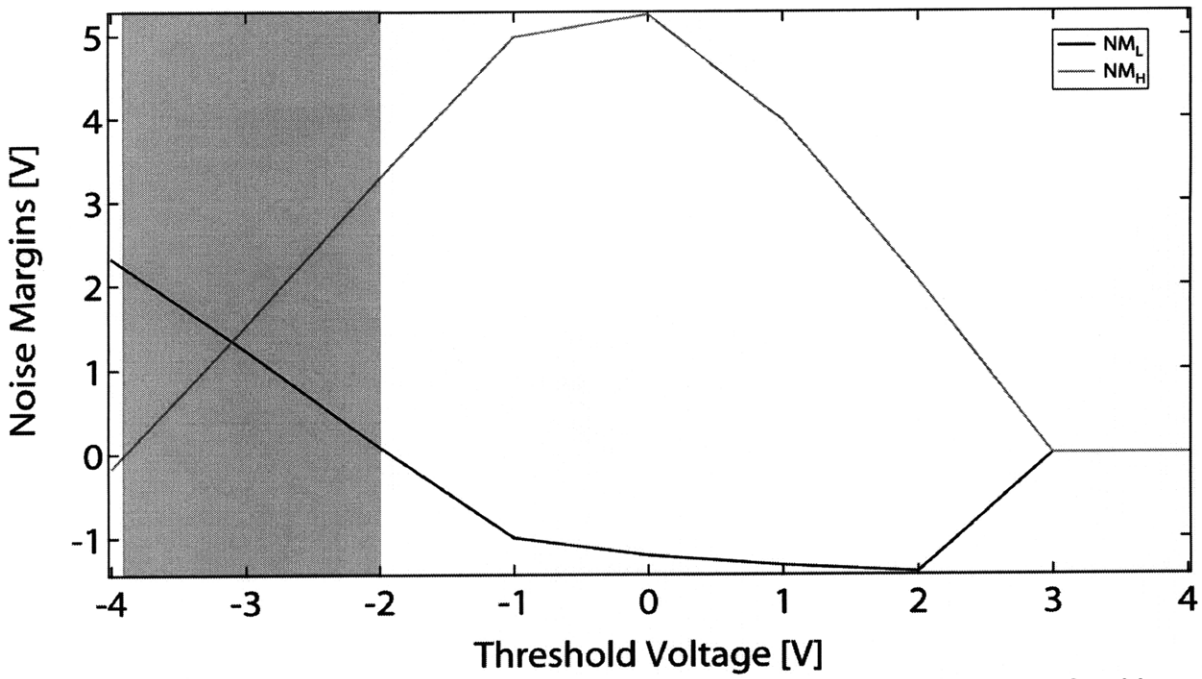


Figure 3-6: Noise margins for diode loaded inverter, V_{DD}=10 V, device ratio=100:1. Area of positive noise margins indicated by blue rectangle.

The inverter characteristics with diode loads can be improved by adding a level-shifter stage, at the expense of increasing circuit complexity and area. OTFT inverters have been demonstrated in literature with marginally improved noise margins by using this approach, usually by using two power supplies [5]. Below we demonstrate how significantly noise margins can be improved with the addition of an ideal level-shift stage.

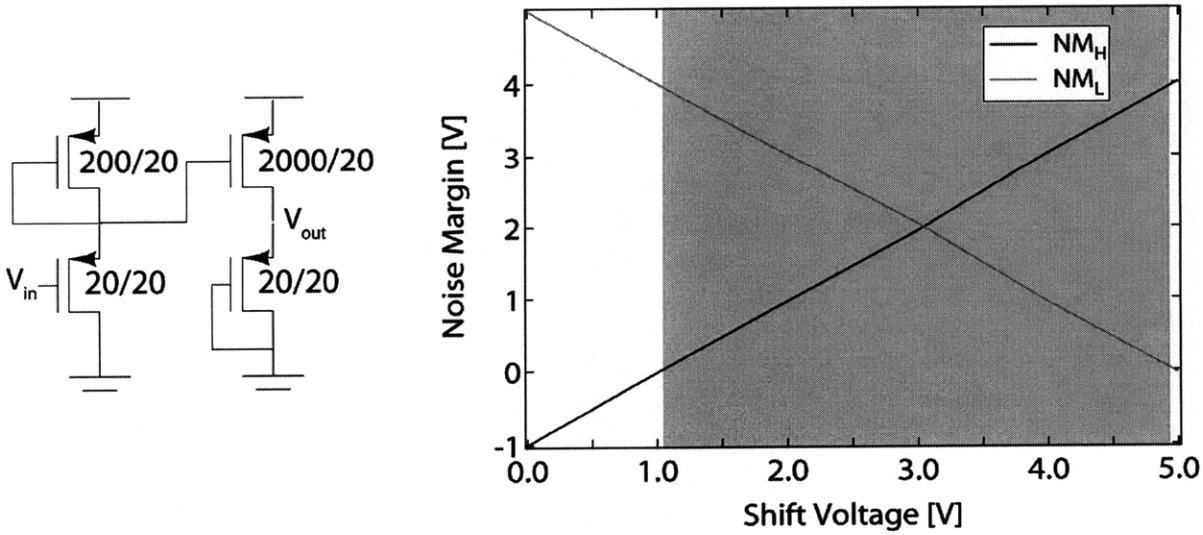


Figure 3-7: Noise margins for diode loaded inverter with ideal level shifter, V_{DD}=10 V, device ratio=100, V_T=-1V. Area of positive noise margins indicated by blue rectangle.

For the diode-loaded inverter, the level shifter is implemented with a source follower stage (Figure 3-8). Unfortunately, using a diode as the load for a source follower results in poor characteristics. Ideally, a source follower behaves as a voltage buffer, with gain of 1 V/V. Going through the small signal analysis, one finds that the voltage gain of this circuit is as follows.

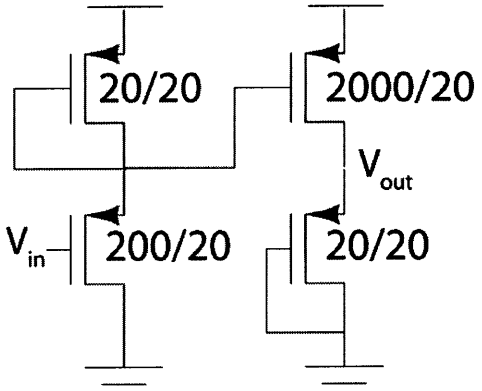


Figure 3-8: Two stage inverter consisting of diode-loaded source follower and common source.

$$A_v = \left(\frac{g_{m,driver}}{\frac{1}{r_{o,driver} \parallel 1/g_{m,load}} + g_{m,driver}} \right) \approx \frac{g_{m,driver}}{g_{m,load} + g_{m,driver}} \qquad (3\text{-}4)$$

One would want to make the load much smaller than the input device, to lower g_m of the load. Doing so affects the large signal characteristics. In general, the source follower provides a small level shift if one wants the gain to be 1.

Overall, the level shifted diode-load was not found to provide any benefit in noise margins. Positive noise margins could not be obtained for V_{DD}=10 V, regardless of the device ratios in each stage.

3.2.3 Zero-V_{GS} Inverter

Instead of shorting the gate to drain, resulting in a diode load, we now investigate shorting the gate to source, creating a zero-V_{GS} load. This load behaves like a current source, and provides improved gain and noise margins due to its higher output resistance. This approach was commonly used in silicon NMOS technology in the 1970's, and has also been demonstrated in III-Vs [6,7]. The gain of the zero-V_{GS} inverter is given by the following equation.

$$A_v = -g_{m,driver} x \left(r_{o,load} \parallel r_{o,driver} \right) \tag{3-5}$$

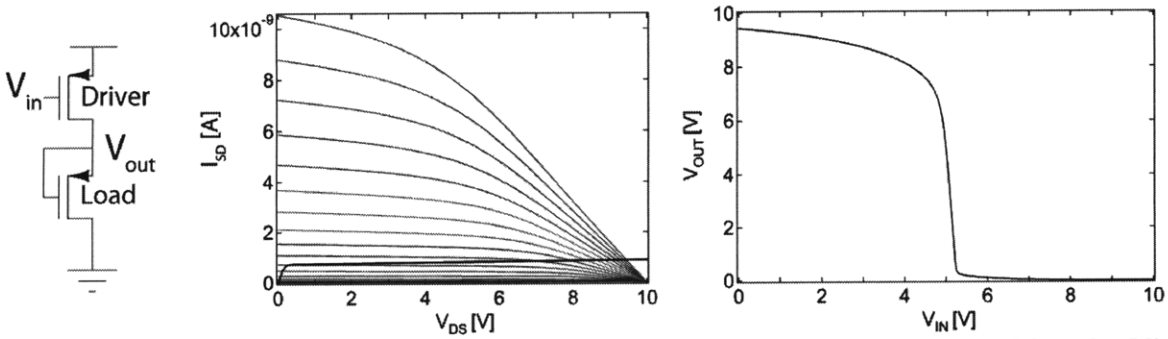


Figure 3-9: Zero-V_{GS} loaded inverter, load line analysis, inverter output curve extracted from load line analysis. W/L load=driver*3800. V_{DD}=10 V

In addition to having higher gain, the zero-V_{GS} load also allows one to size the driver and load such that the trip point is located at $V_{DD}/2$, which we could not do for the diode-loaded inverter case. The only way to have a diode loaded inverter trip at $V_{DD}/2$ is for both devices to have the same W/L, which would provide a maximum gain of -1.

For the example in Figure 3-9, V_T=-1, and the ratio of the load W/L to the driver W/L is 3800. As expected, the noise margins are superior to the diode-loaded case, and NM_H=2.6 V, NM_L=4 V.

We can also investigate the noise margins as a function of V_T to find the robustness of the topology. In this simulation, the threshold voltages of both devices in the inverter are equal, and are swept from -3 V to 3 V. At each V_T, the inverter load sized such that its trip point is at $V_{DD}/2$=5 V, to maximize noise margins. The noise margins are found at each V_T.

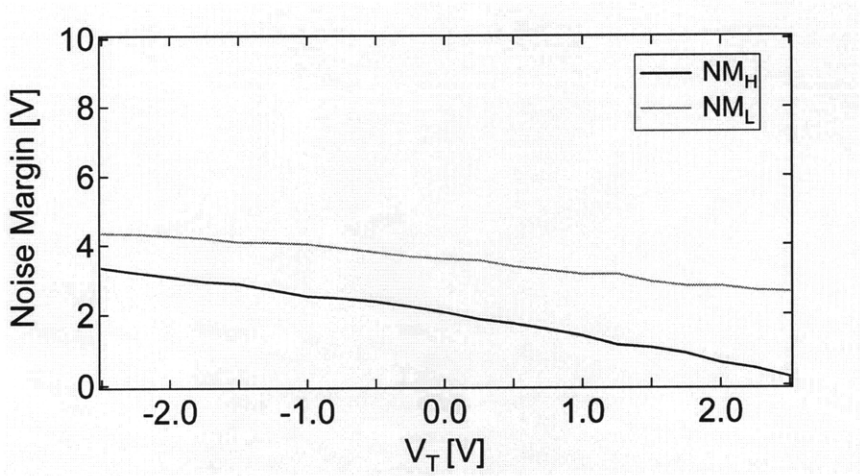


Figure 3-10: Zero-V_{GS} inverter noise margins versus V_T. V_{DD}=10 V. Positive noise margins are achieved for the entire range of V_T's shown.

The simulation results indicate that the zero-V_{GS} topology will exhibit positive noise margins until a V_T of approximately 2.5 V. Noise margins degrade as the V_T becomes more positive for two reasons: the gain decreases because of higher current through the inverter, and second, V_{OH} moves lower, due to both devices being more strongly "on" at V_{IN}=0. The latter is simply a consequence of using a zero-V_{GS} load.

Comparing the results pictured in Figure 3-10 with Figure 3-6, we observe that the zero-V_{GS} inverter has higher noise margins, and a much wider range of V_T's over which positive noise margins are obtained. For these reasons, we will focus our attention on the zero-V_{GS} load as our topology of choice.

3.3 *Effect of Dual V_T and V_{DD} on Circuit Design*

One drawback of zero-V_{GS} OTFTs circuits is the large size required of the load device to achieve positive noise margins [8]. If the inverter trips at $V_{DD}/2$, the V_{SG} on the driver device is $V_{DD}/2$, and the V_{SG} of the load is of course 0. For the load to be sufficiently strong to pull down, the width of the load must be sized very large. This is also exacerbated by the fact that the OTFT is a greater-than-square law device. The performance improvement of a dual V_T process has been speculated in literature [5].

Below, we plot the required ratio of the load W/L to the driver W/L, at a V_{DD} of 10 V.

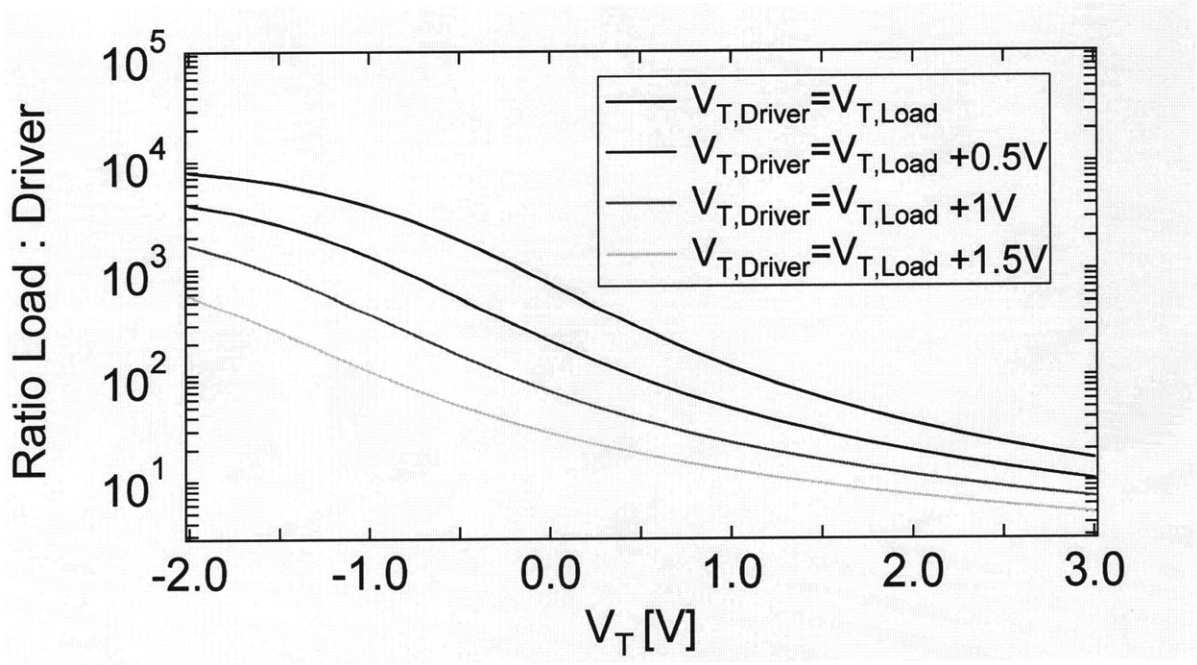


Figure 3-11: Ratio of load W/L to driver W/L to achieve $V_M=V_{DD}/2$.

We also plot the required ratio versus V_T if we introduce a shift in the V_T between the driver and load. By making the load have a more positive V_T (i.e. more depletion-mode) it can sink more current at zero-V_{GS}, therefore decreasing the required width of the zero-V_{GS} device.

In addition, lowering V_{DD} will give us a number of benefits. First, it lowers the power consumption, and gives a higher gain for the same sized devices, since the current through the inverter is smaller. Second, it decreases the required width of the zero-V_{GS} device, since the driver will have a smaller overdrive at the trip point, making it easier for the load to pull down. This is illustrated in Figure 3-12.

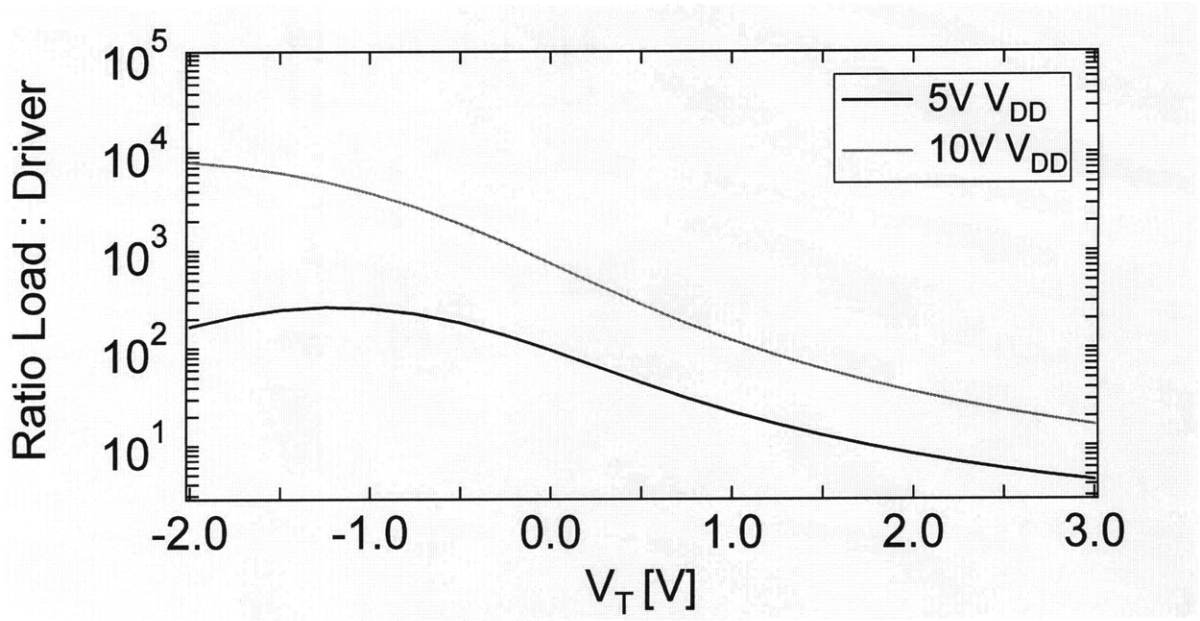


Figure 3-12: Ratio of load W/L to driver W/L for V_{DD}=10 V and 5 V.

In addition, lower V_{DD}'s offer the advantage of improved circuit lifetime. A major challenge to OTFT circuits is bias-stress stability. When a gate to source field is applied across an OTFT to induce accumulation, holes will become trapped at the semiconductor-dielectric interface. This trapped charge results in the I-V curves of the device shifting more negative. Because the trapped charge results in a V_{FB} offset, we can quantify the shift by finding the voltage required to move the stressed I-V back to the initial curve [9]. This voltage is called V_{shift}. Below, we plot the V_{shift} versus time for various V_{GS}.

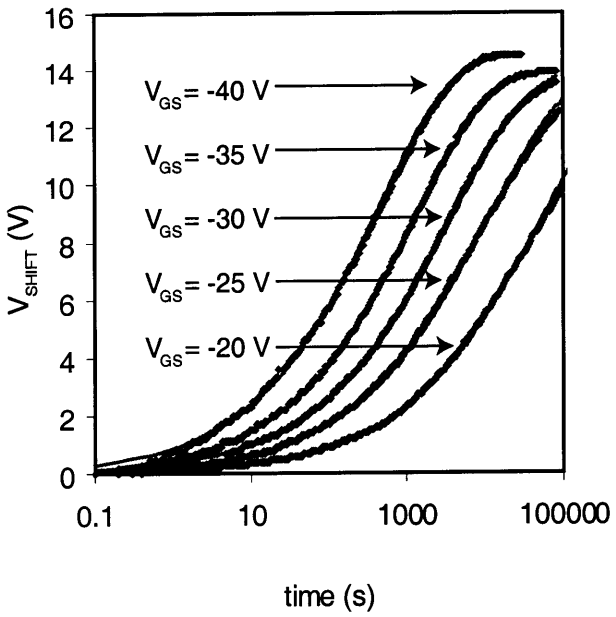
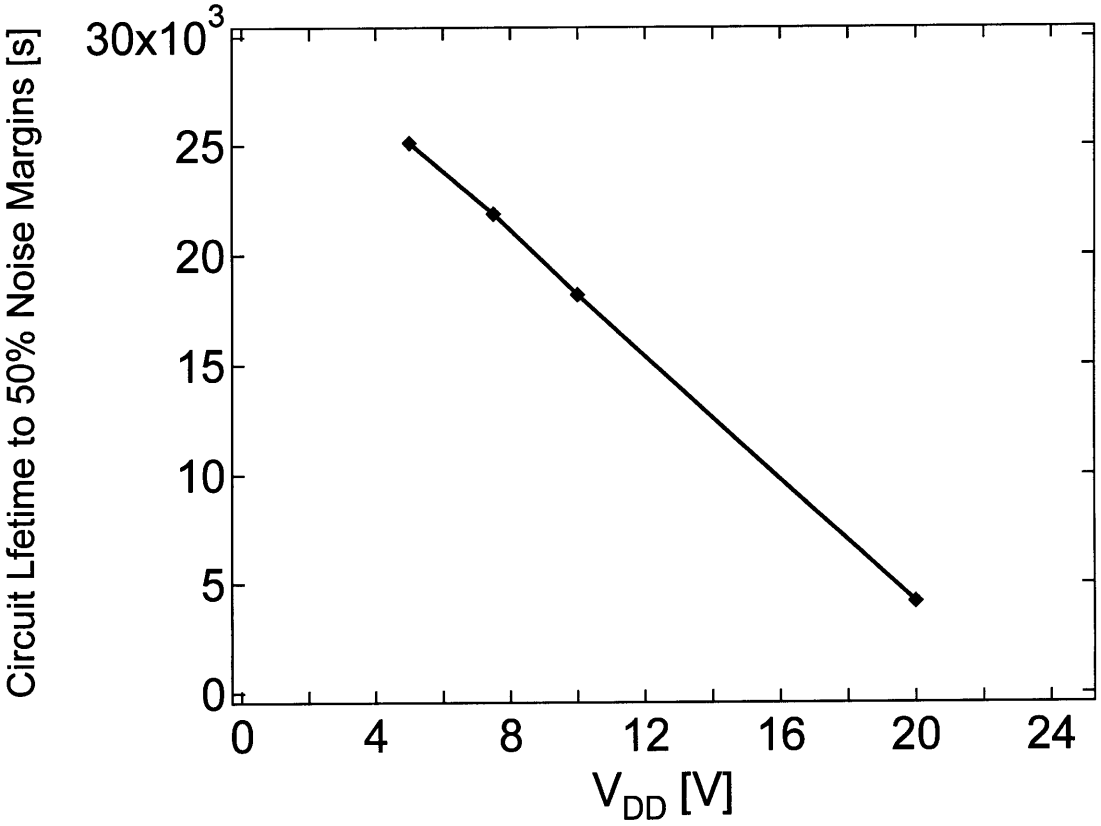


Figure 3-13: V_{shift} versus time for varying V_{GS}. Courtesy of K. Ryu.

We can model the effect of bias-stress stability on the performance of OTFT inverters. In the zero-V_{GS} topology, the load has no external field applied from gate to source, therefore only the driver will degrade from bias stress over time. To find a conservative lifetime of the circuit, we assume a constant V_{SG} across the driver equal to V_{DD}. In addition, we assume that the device is in the linear regime. This is also a conservative assumption, since the bias stress effect is stronger than in saturation due to the increased charge content in the channel. Using these assumptions, we can then find the V_{shift} at which the inverter noise margins degrade by 50%, and when they reach 0.

There are two effects which come in to play as the V_{DD} is reduced. First, the noise margins are decreased as the power supply decreases. This means the V_{shift} the circuit can tolerate becomes smaller. Second, the time dependence of V_{shift} changes as V_{DD} decreases. The amount of time it takes to reach a value of V_{shift} increases as the power supply is decreased, since the gate to source field decreases. The latter effect is dominant, and the circuit lifetime increases as V_{DD} is lowered.

In Figure 3-14, we first plot the circuit lifetime to 50% noise margins, then to 0 noise margins, as computed in the above method, versus V_{DD}. We observe that by lowering V_{DD} from 20 V to 5 V, we improve the circuit lifetime by nearly an order of magnitude. These results give further motivation for OTFT circuit designers to lower the power supply.


Circuit Lfetime to 50% Noise Margins [s]
30x10^3
25
20
15
10
5
0
0
4
8
12
16
20
24
V_DD [V]

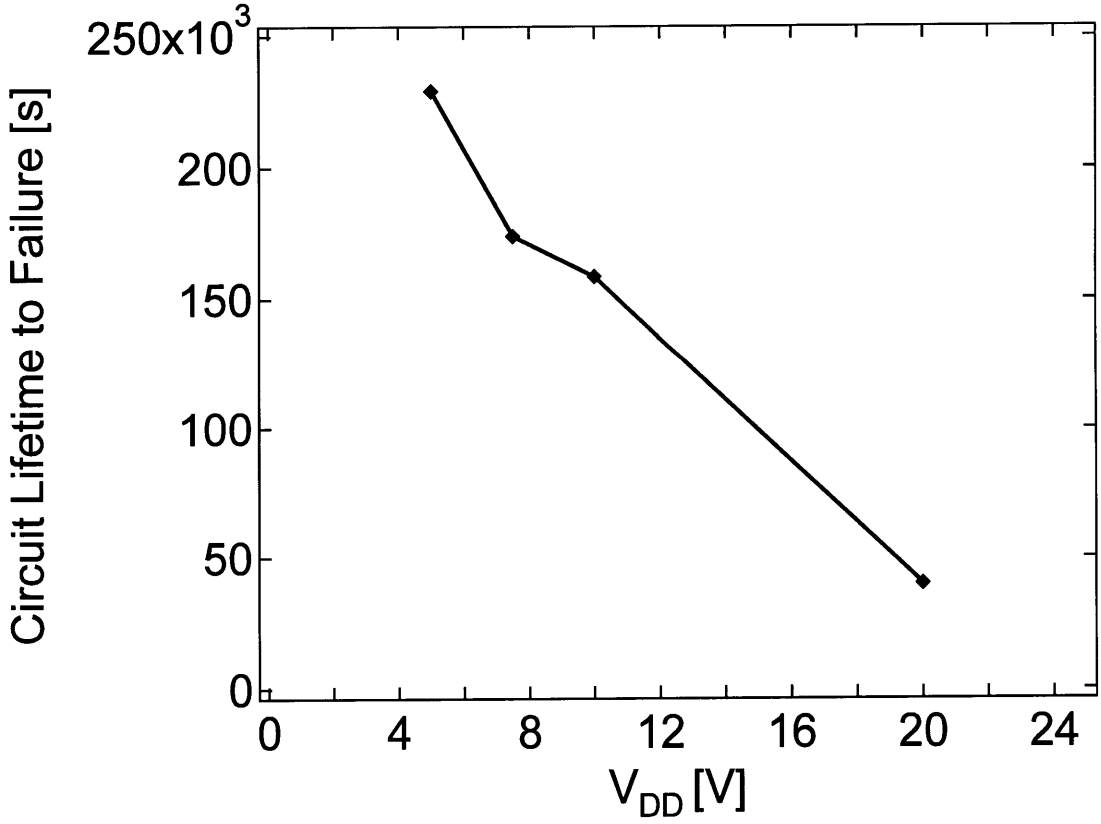

Circuit Lifetime to Failure [s]
250x10^3
200
150
100
50
0
0
4
8
12
16
20
24
V_DD [V]

Figure 3-14: (top) Lifetime of circuit to 50% degradation of noise margins versus power supply. (bottom) Lifetime of circuit to noise margins=0 versus power supply.

3.4 Summary

A DC model for the OTFT current-voltage characteristics was introduced. Good agreement between the model and measured data was found.

This model was implemented in MATLAB for the purpose of analyzing the large signal characteristics of OTFT inverters. It was found that inverters with zero-V_{GS} loads offer significantly higher noise margins than diode-load inverters for a wide range of threshold voltages. Therefore, further investigation concentrated on the zero-V_{GS} topology.

One drawback of the zero-V_{GS} inverter is that the load's width must be very large to pull-down at $V_{DD}/2$. Simulations revealed that a dual threshold voltage technology could significantly reduce the size requirements of the load device.

The case for lower V_{DD}'s was also motivated. Reducing the power supply was found to decrease the width of the load necessary for high noise margin inverters. By combining the simulation tool with bias stress data, the lifetime of the circuits was also forecasted. Lowering the power supply from 20 V to 5 V was shown to increase the inverter lifetime, defined by the percent degradation of noise margins, by ~6x.

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Chapter 4 Dual Threshold Voltage Process

A dual threshold voltage technology could provide significant area and speed savings for organic circuits. In this chapter, a near-room-temperature process (≤95°C) that produces integrated dual V_T PMOS devices is presented. The two different V_T's are enabled by using different gate metals. A low work function metal (aluminum) was used as the gate of the low V_T device (i.e. enhancement-like), and platinum was used as the gate of the high V_T device (i.e. depletion-like). The additional gate layer requires one more mask step compared to the conventional process described in Chapter 1.

Devices were fabricated and found to have nominally the same mobility as the conventional single V_T process. Other device parameters such as $R_{contact}$ and the subthreshold slope were also observed to be in line with the standard process.

The Al and Pt gate devices were observed to have nominally identical current-voltage characteristics, although shifted from each other by an amount we term the ΔV_T. The dual V_T process, which uses a thin (120 nm) parylene-C gate dielectric, is measured to have a ΔV_T of 0.6 V, consistent over multiple wafers.

It was found that lift-off processed metal gates was necessary to ensure a reproducible ΔV_T. Other processes using etched gate metals are summarized. All processes involving etched metals exhibited no ΔV_T, which suggests contamination of the metal surface during the additional process steps.

4.1 Introduction and Literature Review

Figure 4-1 shows a band diagram schematic of a generic metal-insulator-semiconductor system. For the standard photolithographic process, the gate is Au, the dielectric parylene-C, and the semiconductor pentacene. We assume the pentacene is intrinsic, implying that its Fermi level is in the middle of the bandgap at 4.15 eV. All energy levels are referenced to the vacuum level.

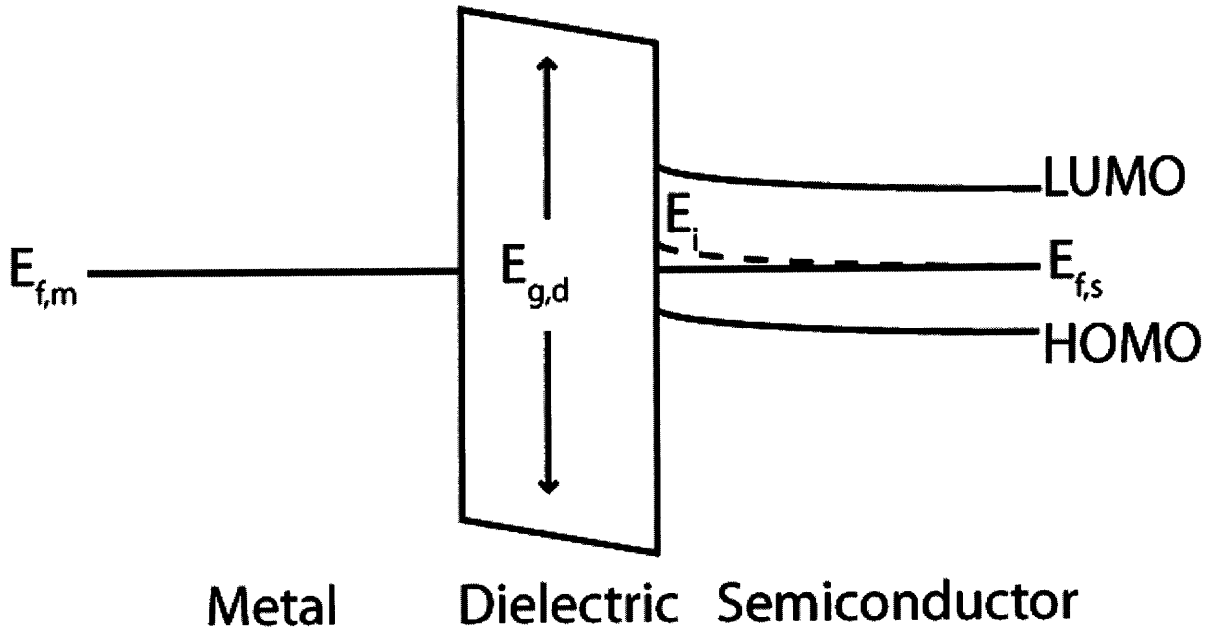

Figure 4-1: Metal, dielectric, semiconductor band diagram. Here, $E_{f,m}$=5.10 eV (Au), and $E_{f,s}$=4.15 eV (pentacene). V_{SG}=0 V.

Since the gate and semiconductor are typically of different potentials, when these three layers are put together, there will be some charge at the gate-dielectric interface, and at the dielectric-semiconductor interface. This is the case for the example pictured in Figure 4-1. Therefore, an electric field will exist in the dielectric. If we apply a voltage to the gate, we can change the charge content at both of these locations. At some particular voltage on the gate, there will be no charge at the dielectric-semiconductor interface, and no charge at the gate-dielectric interface. Therefore, no field is dropped across the dielectric, and likewise there is no field in the semiconductor layer. This gate voltage is called the flat band voltage, and is described by the following equation for this structure [1]. In Figure 4-1, a positive voltage on the gate would be necessary to achieve flat band.

$$V_{FB} = \left(\phi_{gate} - \phi_{semiconductor}\right) - \frac{1}{\varepsilon}\left(\int_0^t \left[\int_0^x \rho_o(x)dx\right]dx\right) \tag{4-1}$$

Nominally, the flat band voltage is the difference between the gate and semiconductor potentials, but any fixed charge throughout the dielectric must be accounted for and is reflected in the last term. In practice, fixed charge in the dielectric is very hard to distinguish from fixed charge at the semiconductor-dielectric interface [1]. Equation 4-1 can be simplified by lumping together all the fixed charge in the dielectric and treating it as if it were fixed sheet charge at the interface. This term is Q_I, and is in units of C/cm^2.

$$V_{FB} = \left(\phi_{gate} - \phi_{semiconductor}\right) - \frac{Q_I}{C_{ox}} \tag{4-2}$$

We will use this equation to describe the flat band voltage in the OTFT system. However, since OTFTs operate in accumulation, literature typically refers to this voltage as the threshold voltage (V_T) since it is at this voltage when OTFTs "turn on". To be consistent with organic literature, the quantity described in Equations 4-1 & 4-2 will be called V_T.

Equation 4-2 indicates there are three ways to change the V_T – by altering the gate potential, semiconductor potential, and adding or altering the interface charge. A survey of literature reveals a handful of papers which have changed the threshold voltage in OTFTs through the latter two of these approaches.

Cantatore et al., use a spin-cast pentacene precursor, and can shift the transfer curves of the devices by adjusting the quantity of a proprietary chemical in the spin-cast solution [2]. The resulting devices have V_T's shifted ~2.5 V more positive, and a degradation of the subthreshold slope. An illustration of the I-Vs before and after is pictured in Figure 4-2. It is unclear if they are only modulating $\varphi_{semiconductor}$, and not also increasing the interface charge. This process only produces a single V_T device, albeit more "depletion-like". As shown in Chapter 3, a more positive V_T will allow for a smaller required width of the zero-V_{GS} load.

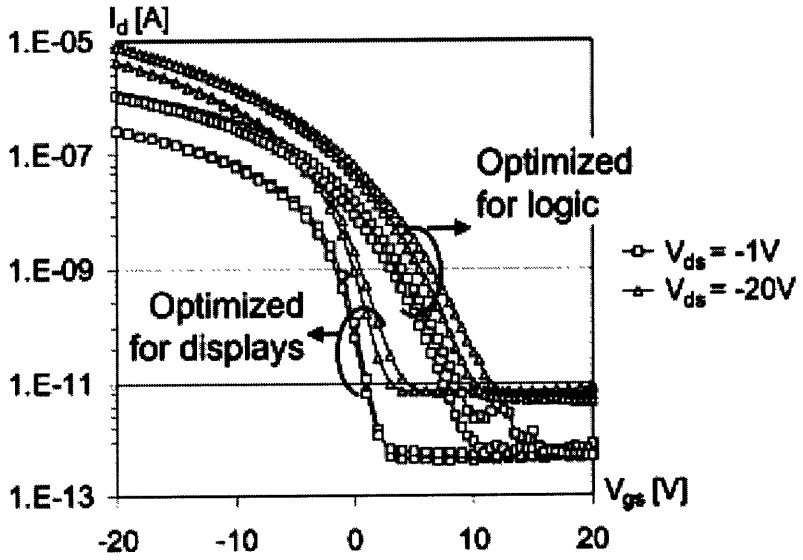

Figure 4-2: Shifting of I-Vs by addition of precursor chemicals [2].

The drawbacks of this approach are as follows:

1. Produces only a single V_T device.
2. Relies on spin-casting the semiconductor, and is incompatible with thermally evaporated processes.
3. Achieves a positive V_T by degrading the electrical performance of the device.
4. Likely adds interface charge, which may be an uncontrollable/unreproducible.

Wang et al., propose a method to shift the V_T by purposefully introducing fixed charge at the interface [3]. Parylene-C is used as the gate dielectric, and is exposed to reactive oxygen in

the form of either oxygen plasma or ozone. This step is done prior to pentacene deposition. Exposure of the organic dielectric to reactive oxygen results in an increase in Q_I. Pentacene is then evaporated onto the damaged surface. The resulting devices should have threshold voltage shifts proportional to Q_I/C_{ox}. In this case, the change in V_T is greater than 100 V, due a negative sheet charge density of $Q=1.3x10^{13}$ cm^{-2} the interface. This number corresponds to fixed charge on ~13% of every surface site. The output curves of treated and un-treated devices are pictured in Figure 4-3.

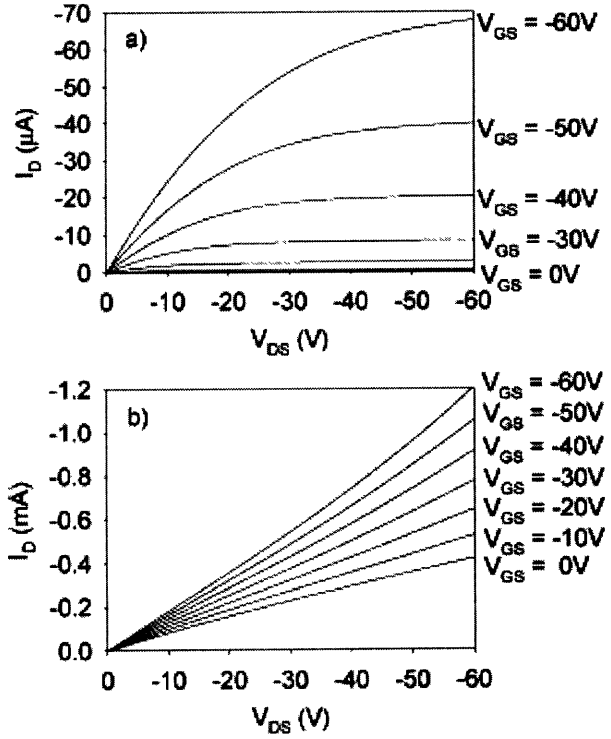

Figure 4-3: Creation of extreme depletion devices by oxygen plasma treatment of parylene dielectric [3]. (Top) Without plasma treatment. (Bottom) with plasma treatment.

The oxygen plasma process reported creates a single V_T device, but could be modified to produce two V_T's, by masking the desired areas with photoresist during oxygen plasma. Unfortunately, the shift in V_T is too large to create depletion-mode transistors and the resulting devices behave like resistors. These devices could be used as resistor loads, though resistor-load inverters have worse noise margins than current-source loads. The drawbacks of this approach are summarized below.

1. Creates resistors, not depletion devices.
2. Shift in V_T dependent on gate capacitance. The parylene thickness is poorly controlled by the existing specialty coating systems deposition tool.
3. Unproven reproducibility.

Although the oxygen plasma approach by *Wang et al.* may be difficult to integrate into a controllable process, it proves the feasibility of affecting the OTFT characteristics by treating the dielectric surface prior to semiconductor deposition.

Lastly, *Takamiya et al.* patterned a back gate on each transistor [4]. This extra terminal enables control of the semiconductor potential from the backside. By applying a positive back gate voltage, one moves the semiconductor potential toward the LUMO, making it harder to accumulate. Likewise, a negative back gate voltage moves the semiconductor potential towards the valence band, making the device easier to turn on. Applying a voltage to the back gate has much the same effect as adjusting the bulk potential in a silicon MOSFET The effect of changing the back gate voltage is shown in Figure 4-4.

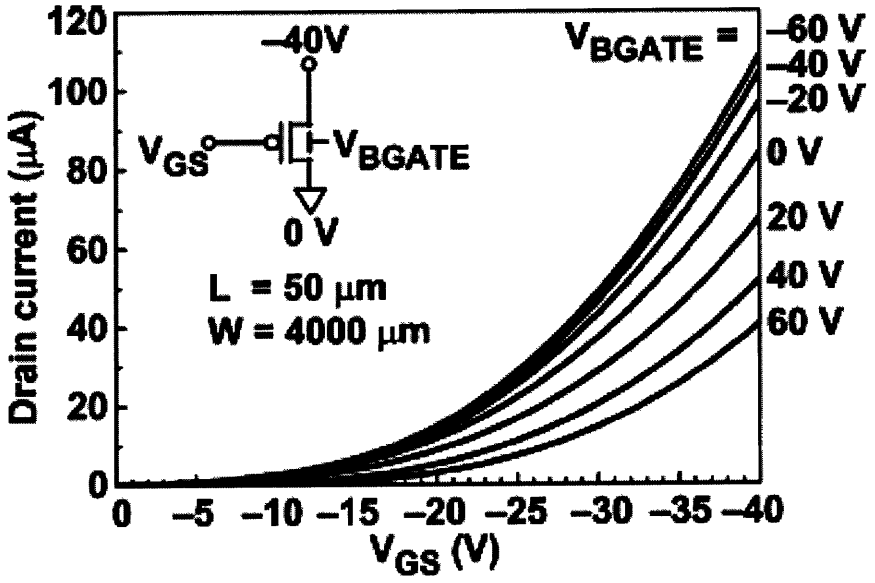

Figure 4-4: Control of device characteristics through back gate terminal [4].

Although this method was shown to increase the noise margin of inverters, the approach has a number of disadvantages.

1. The top surface of pentacene films is of rougher texture than the bottom surface. To achieve reproducible back gate control, one needs to control the morphology and interface of two surfaces.
2. Adds a second power supply.
3. It increases processing complexity.

In the next section, we introduce a process that produces dual threshold voltage devices without degradation of device characteristics, or introduction of fixed charge. Dual V_T devices are patterned with the addition of only one extra mask step. Threshold voltage modification is achieved by changing the gate metal work function. This is the first report of V_T modulation in OTFTs by altering the gate metal.

4.2 Process Design

Referring back to Equation 4-2, one sees that a change in the gate's potential will linearly change the threshold voltage. First, we assume that the semiconductor potential, $\varphi_{semiconductor}$, and the fixed charge, Q_I, are uniform across the wafer. This should be a reasonable assumption, since both devices' dielectric and semiconductor layers are processed at the same time.

Therefore, by changing the gate metal we should obtain a shift in threshold voltages between the two devices, ΔV_T. Ideally, we would want to maximize ΔV_T, but metal work functions vary by at most a few eV. Table 4-1 lists the work functions of some common metals.

Metal	Work function [eV]
Ce	2.10
K	2.30
Hf	3.98
Ta	4.25
Ag	4.26
Al	4.28
Ti	4.33
Zn	4.35
Co	5.00
Au	5.10
Pd	5.12
Ni	5.15
Pt	5.65

Table 4-1: Common metals and their work functions.

Unfortunately, low work function metals like cesium (Ce) and potassium (K) are extremely reactive in atmosphere, and are therefore not suitable for use as gate electrodes. Hafnium (Hf) would be an ideal choice as the low work function metal, but was not available in any deposition tool in TRL. Therefore, Al and Pt were chosen as the two gate metals. The proposed band diagram of the gate-dielectric-semiconductor structures is shown below. Theoretically, one would expect a flat band voltage difference of ~1.3 V between the two devices.

The band diagrams below show the case for aluminum and platinum gates. All potentials are referenced to the vacuum level. The pentacene HOMO is 5.2 eV, and the LUMO 3.1 eV [5]. It is assumed to be intrinsic, therefore its Fermi level is in the middle of the bandgap at 4.15 eV. The pentacene-parylene HOMO offset was measured by ultraviolet photoelectron spectroscopy (UPS) to be ~ 2 eV. The parylene bandgap has been reported to be 4.4 eV to 6 eV [6,7].

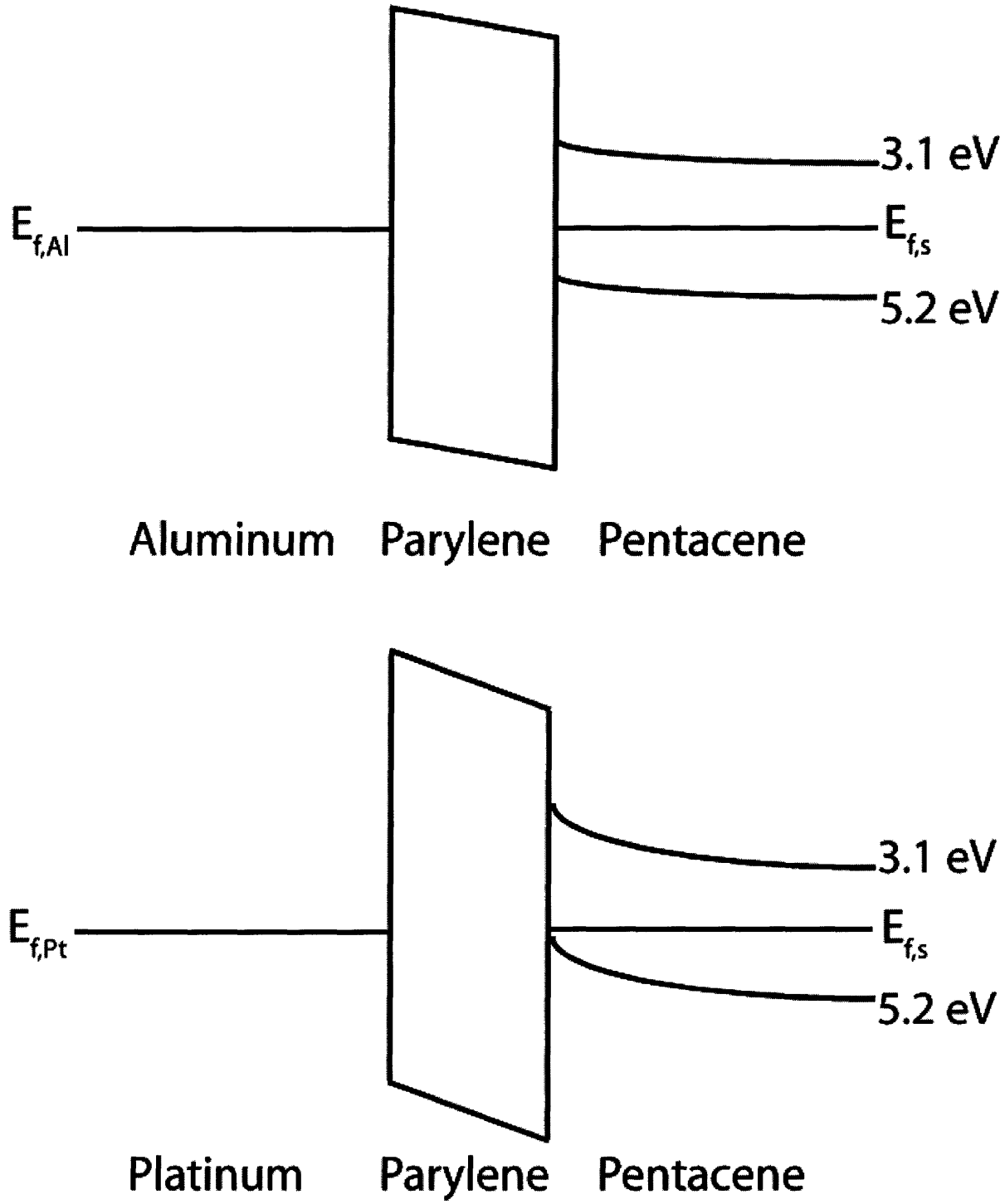

Figure 4-5: Metal, insulator, semiconductor band diagrams with Al and Pt gates. The Fermi level of aluminum, $E_{f,Al}$=4.28 eV, and $E_{f,Pt}$=5.65 eV. V_{SG}=0 V.

4.3 *Integrated Process Flow*

An illustration of the process steps is shown in Figure 4-6. All processing was done in the Technology Research Laboratory in MTL.

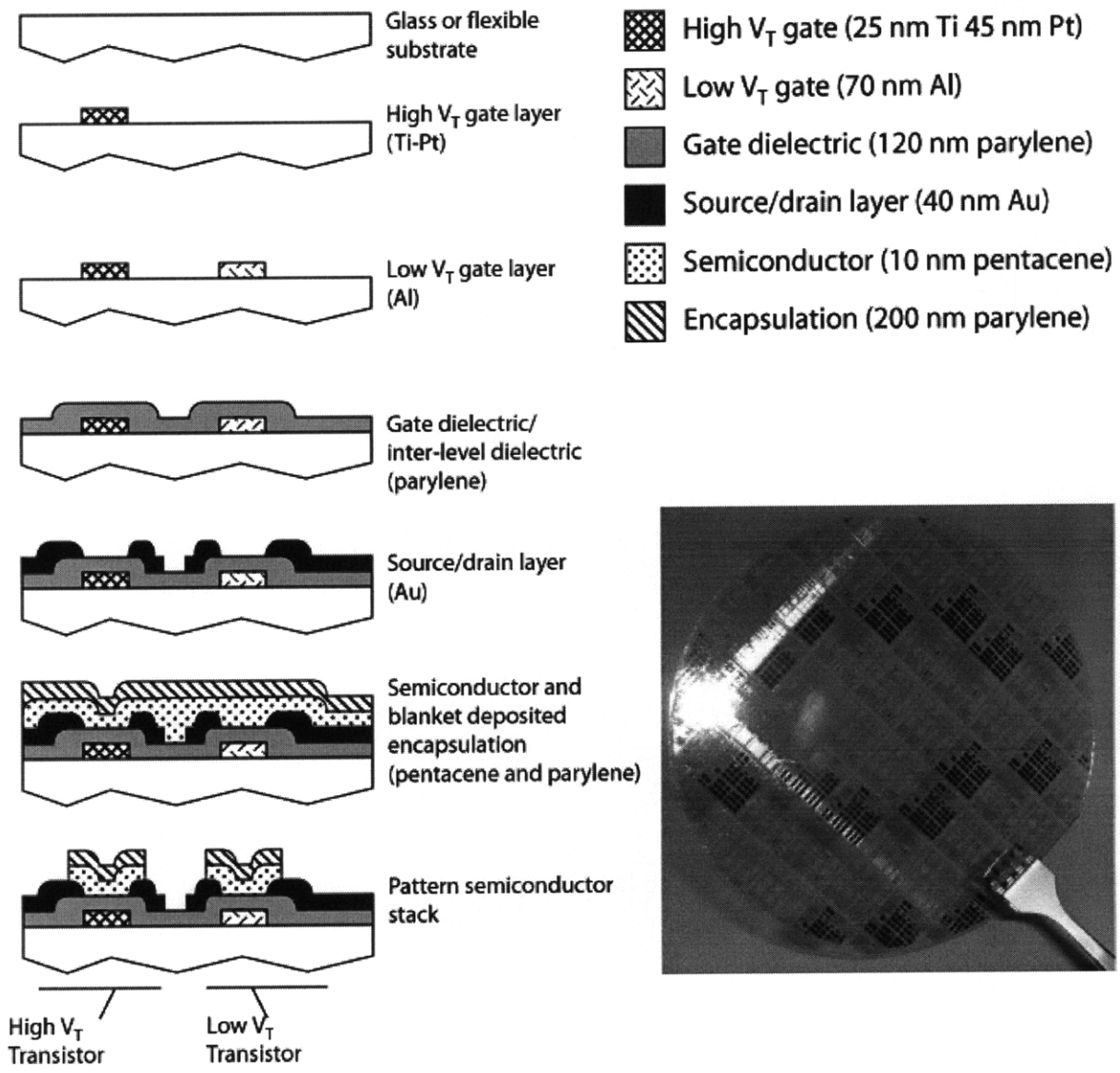

Figure 4-6: Fabrication steps for dual V_T process, and finished 4" wafer.

Four inch borosilicate glass wafers were immersed in piranha solution (3:1 H_2SO_4:H_2O_2) for 10 minutes. Image reversal resist AZ5214E was spin cast for 5 seconds at 500 RPM, 5 seconds at 750 RPM, and 30 seconds at 2000 RPM. Wafers were prebaked at 88°C for 30

minutes in a nitrogen backfilled oven. This time and temperature were found to improve pattern yield, compared with the previously used 20 minutes in 95°C. In the author's experience, the photolithography step is critical for the metal depositions to adhere. The high V_T gate mask was exposed for 1.4 seconds with hard contact. Wafers were postbaked for 30 minutes at 88°C in the same N_2 oven. Photolithography was completed by flood exposing for 48 seconds and developing for 2:20 minutes. Wafers were de-scummed in a barrel asher for 10 minutes at 1000 W.

25 nm of titanium (for adhesion), and 45 nm of platinum were electron beam evaporated. After deposition, wafers were placed face-down in acetone, and left overnight. Finally, wafers were placed in fresh acetone and sonicated for 5 minutes. This step was necessary to completely remove any unwanted metal.

Photolithography for the low V_T gate was performed in exactly the same manner. Metallization consisted of 70 nm of e-beam evaporated aluminum, and liftoff was done following the same steps as above. After removal from acetone, the wafers were rinsed with de-ionized water, then spin-rinsed-dried (SRD). They were immediately loaded for parylene-C deposition. 120 nm of parylene-C was deposited via hot filament CVD.

All subsequent steps are the same as the standard single V_T process described in Chapters 1 & 2. Via holes were patterned using standard positive photoresist and an etch in oxygen plasma. Photoresist was stripped by immersing and agitating in microstrip for 10 minutes, followed by SRD. 40 nm of gold was e-beam evaporated, and patterned with positive photoresist and a wet etch in 5:1 DI water: Transene TFA gold etchant. Wafers were again stripped in the same way as the previous layer.

After SRD, wafers were loaded into the pentacene thermal evaporator. 10 nm of pentacene was evaporated at rate of 0.6 nm/min at a pressure of $5x10^{-7}$ torr. The semiconductor layer was then encapsulated with 200 nm of parylene-C. Another positive photo step and oxygen plasma etch for 180 s isolated the active area.

4.4 Characterized Devices

Devices were characterized in the same manner as mentioned in Chapters 1 & 2. Figure 4-7 shows the transfer characteristics of two W/L=200 μm/15 μm Al and Pt gate devices. No measurable difference in C_{ox}, subthreshold slope, or mobility between the Al and Pt gate transistors was observed. There was no significant difference found in the device parameters (e.g. mobility, $R_{contact}$), compared with the standard Au gate, single V_T process.

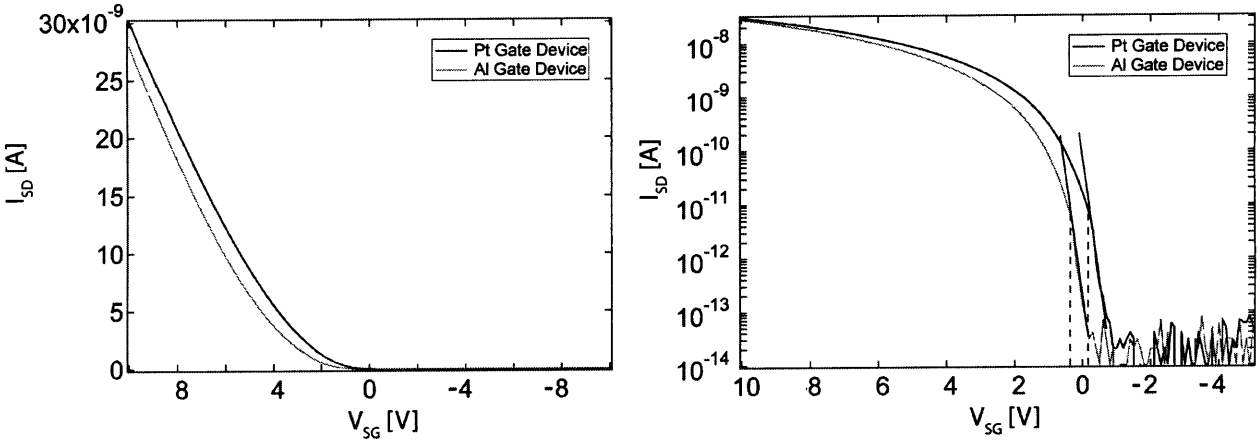

Figure 4-7: Linear and semi-log transfer characteristics for W/L=200 μm/15 μm devices, V_{SD}=-1V. $V_{T,Al}$=-0.5 V, $V_{T,Pt}$=+0.1V

The aluminum and platinum gated devices' I-Vs were found to be nominally identical, although shifted along the V_{SG} axis. This shift we call ΔV_T, and a ΔV_T of 0.6 V was consistently reproduced over numerous wafers. We extract the absolute V_T's by fitting a straight-line to the subthreshold region, and noting the V_{SG} at which the I-V pulls away. This process is pictured in Figure 4-7. The absolute V_T's and ΔV_T's for three wafers are summarized in Table 4-2. These wafers were processed in separate lots.

Parameter	Wafer 1	Wafer 2	Wafer 3
Al Gate Mean V_T	-0.43 V	-0.46 V	-0.72 V
Al Gate Std. Dev. V_T	0.10	0.09	0.15
Pt Gate Mean V_T	+0.23 V	+0.08 V	-0.16 V
Pt Gate Std. Dev. V_T	0.10	0.08	0.15
Mean ΔV_T	+0.65 V	+0.54 V	+0.56 V
Std. Dev. ΔV_T	0.06	0.05	0.09

Table 4-2: Threshold voltage statistics across three wafers run using the dual V_T process.

4.5 Effects of Processing on ΔV_T

A number of variations on the standard process described in the previous section were tried, which used chemical etches to pattern the gate layers, instead of the lift-off described earlier in the chapter. None of these etched processes showed a reproducible ΔV_T.

The first variant switched the order of gate processing, and chemically etched the aluminum layer. This process was investigated because the omission of one liftoff step would reduce processing complexity. The process flow is shown in Figure 4-8.

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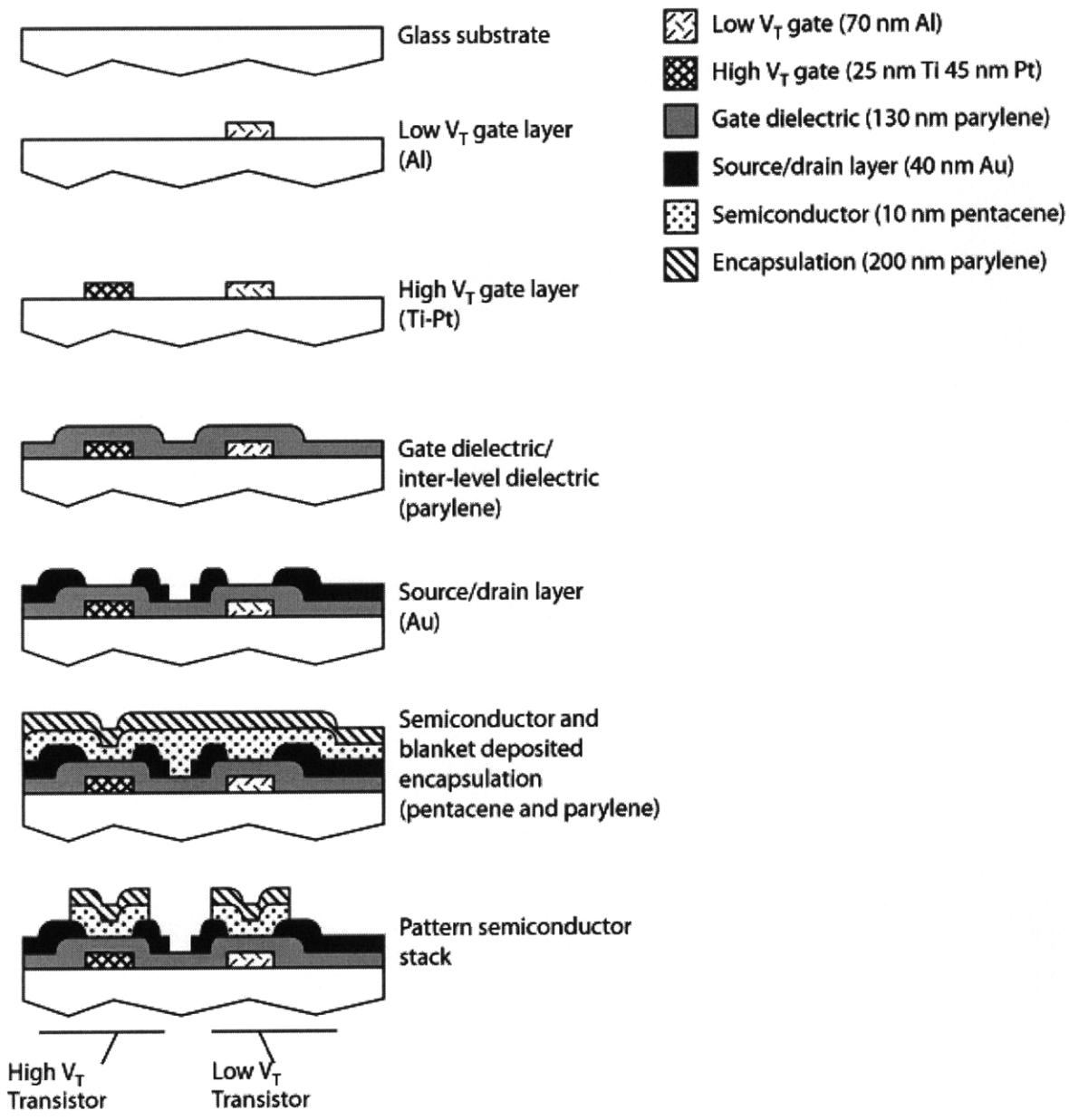

Figure 4-8: Process for etched low V_T gate.

After the aluminum layer was deposited, positive resist was spin-cast, exposed, and developed. The aluminum was then patterned by immersing the wafers in Transene Type A aluminum etchant (80% by weight H_3PO_4, 5% HNO_3, 5% CH_3COOH, 10% H_2O) for 1.5 minutes. The positive resist was then stripped with microstrip, and rinsed with DI water.

AZ5214E image reversal resist was then spin cast, exposed, and developed. After descum, 25 nm of Ti and 45 nm of Pt was e-beam evaporated, and lifted off in acetone. Subsequent processing was done in the same manner as the lift-off dual V_T process.

Compared to the lift-off dual V_T process, the aluminum layer underwent a number of additional process steps. These additional steps seen by the metal layer are summarized:

1. Positive photo resist, and developer
2. Chemical etch in phosphoric, acetic, nitric acids
3. Solvent bath of microstrip
4. Negative photo resist, and developer
5. Baking / UV exposure

The absolute V_T, and ΔV_T were extracted for three fabricated wafers. These results are shown in Table 4-3.

Parameter	Wafer 1	Wafer 2	Wafer 3
Al Gate Mean V_T	-0.12 V	0.03 V	-0.12 V
Al Gate Std. Dev. V_T	0.20	0.19	0.18
Pt Gate Mean V_T	+0.04 V	+0.00 V	+0.10 V
Pt Gate Std. Dev. V_T	0.15	0.12	0.10
Mean ΔV_T	+0.08 V	-0.03 V	+0.22 V
Std. Dev. ΔV_T	0.08	0.17	0.16

Table 4-3: Threshold voltage statistics across three wafers run using the etched Al dual V_T process.

A second process was investigated, using an "etch-back" gate process, which required no lift-off steps. The process' goal was to use two gate metals which could be easily chemically etched. Both metals were deposited at once. The top metal layer was patterned as the first gate. The adhesion layer below was then patterned and served as the second gate electrode.

Since it cannot be easily chemically etched, platinum was unavailable as the high V_T gate, and gold was substituted. Also, the high V_T gate must also have a selective etch against the high V_T gate metal, and serve as an adhesion layer between glass and the other gate metal. To satisfy these requirements, titanium was used as the second gate metal.

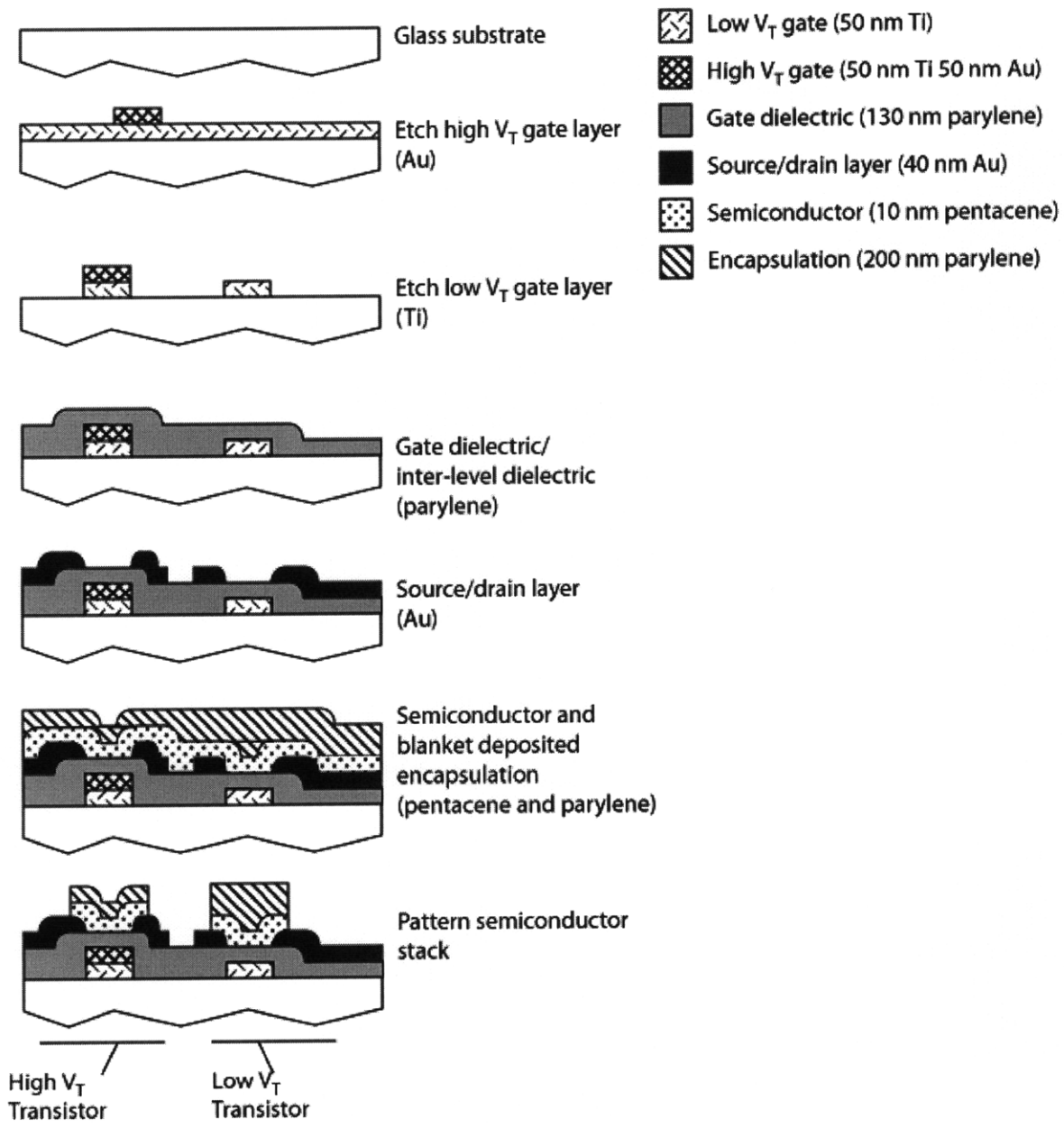

Figure 4-9: Etch-back process using titanium and gold gates.

After a piranha clean, 50 nm of titanium was e-beam evaporated, followed by 50 nm of Au. Both layers were deposited during the same run, without breaking vacuum. Positive photo resist was spun on the gold, baked, exposed, and developed. The gold layer was etched by immersion in 5:1 DI water to Transene TFA for 1:45 minutes. This etch is selective to gold, and will not attack the underlying titanium layer. The photoresist was removed by microstrip. Positive photo resist was again spin cast, baked, exposed, and developed. The titanium layer was etched in 30:1 H_2O: buffered oxide etch (6:1 40% NH_4F 60%H_20, 49%

HF 51% H_2O) for 1:30 minutes. Photo resist was stripped in microstrip, and wafers were rinsed in DI water and blown dry.

The etch-back process exposes both gates to additional processing steps, compared to the lift-off dual V_T process. To summarize, the gold gate sees these additional steps:

1. Positive photo resist and developer
2. Au etchant
3. Microstrip
4. Buffered oxide etch

The titanium gate sees the following additional processes:

1. Deposition of Au
2. Au etchant
3. Microstrip
4. Positive photo resist and developer
5. Buffered oxide etch

Multiple wafers were fabricated using these processes, and their threshold voltages were extracted. The intra-die ΔV_T was also extracted, and is listed in Table 4-4.

Parameter	Wafer 1	Wafer 2	Wafer 3
Ti Gate Mean V_T	-0.56 V	-0.38 V	+0.4 V
Ti Gate Std. Dev. V_T	0.18	0.24	0.16
Au Gate Mean V_T	-0.56 V	-0.26 V	+0.16 V
Au Gate Std. Dev. V_T	0.15	0.30	0.29
Mean ΔV_T	+0.00 V	+0.14 V	-0.24 V
Std. Dev. ΔV_T	0.10	0.05	0.17

Table 4-4: Threshold voltage statistics across three wafers run using the etched Ti/Au dual V_T process.

4.6 Analysis of ΔV_T

None of the wafers processed by etching exhibited a substantial or reproducible threshold voltage shift. Since the etched processes' metal surfaces see many processing steps, the metal gates surfaces' may be modified resulting in a different surface potential, and therefore V_T. It is well known that the presence of water or other solvents on a metal surface can change the surface potential by 1 eV or more [8-10]. Contamination of the metal surfaces may also lead to poor parylene deposition and the creation of a high density of surface states. The presence of surface states at the metal-dielectric can lead to Fermi level pinning, a phenomenon often observed in CMOS [11].

Depending on the combination of the gate and dielectric materials and processing steps, interface states may exist, causing the observed V_T to be different than that calculated from the intrinsic material work functions. This has been widely reported in silicon literature, and pinning is particularly strong in the case of high-κ dielectrics such as HfO_2. In Figure 4-10, the metal-dielectric band diagram is drawn for the case of a low work function, and high work function metal. Some density of states exists at the interface, with mean energy $E_{extrinsic}$. If $E_{extrinsic}$ is below the metal's intrinsic work function, electrons will transfer from the metal to the extrinsic states, lowering the effective work function of the gate. Likewise, if the metal work function is below the pinning level, holes will be transferred to the extrinsic states, resulting in a higher effective work function. The effective work function therefore depends on the energy of $E_{extrinsic}$, and the density of extrinsic states.

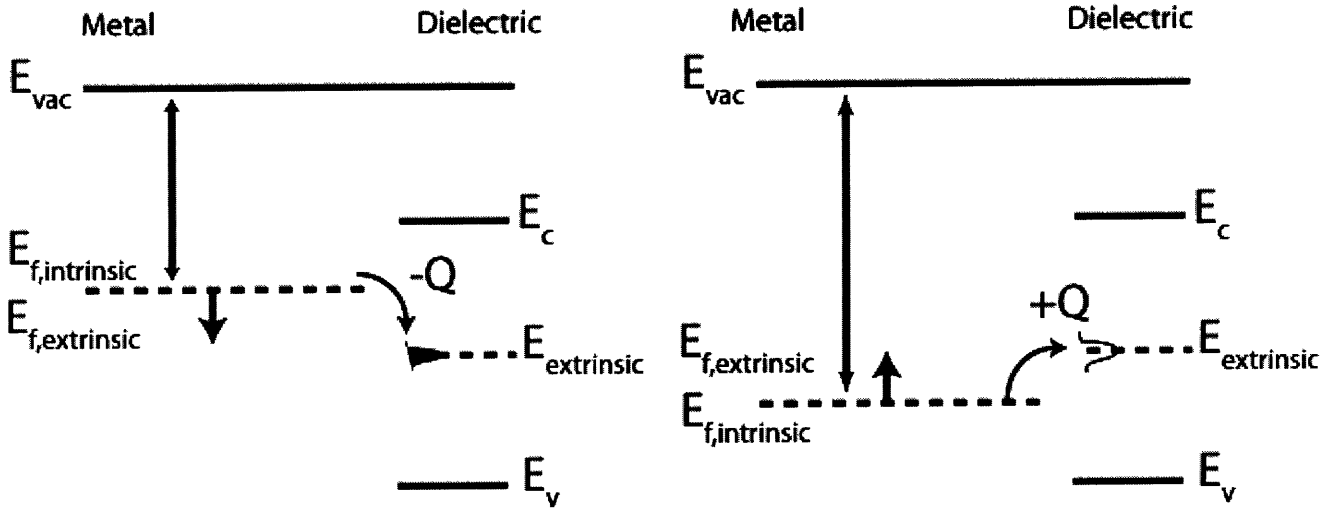

Figure 4-10: Band diagram of metal-dielectric illustrating Fermi level pinning for a low work function gate and high work function gate. After [11].

Further experiments are necessary to conclude Fermi level pinning at the metal-dielectric interface is the cause for the observed ΔV_T's. It is clear however, that exposing the metal surfaces to as few processing steps as possible is essential to observing a consistent and substantial ΔV_T.

4.7 Summary

This chapter introduced an integrated dual threshold voltage technology. Reported techniques for changing the V_T in OTFTs were presented. The benefits of using a dual gate metal process were discussed. A dual V_T process was described, using lift-off to pattern Al and Pt gates. The process adds one additional mask step compared to the standard single V_T process described in Chapter 1. Integrated OTFTs were fabricated and characterized, and found to be nominally identical, except shifted by an amount ΔV_T. The device parameters of dual V_T OTFTs were observed to be no different than those of single V_T devices.

Two other processes were described, which used etching steps to fabricate the metal gates. Multiple wafers were ran on each process. Neither process was found to produce a substantial or reproducible ΔV_T. This behavior was attributed to contamination of the metal surfaces by additional processing steps. The additional processing may also produce surface states between the metal and dielectric, increasing Fermi level pinning and changing the effect work functions of the gates. Other experiments to study the metal-dielectric interface would be necessary to conclusively link processing steps to the cause of the measured ΔV_T.

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Chapter 5 Dual V_T Mixed Signal Integrated Circuits

Analog and digital circuits were designed and fabricated using the dual threshold voltage process flow described in Chapter 4. Record results for organic integrated circuits were measured, including area-minimized logic operating at a 3 V power supply and using picowatts of power. Rail-to-rail ring oscillators were tested and measured to have an oscillation frequency of 1.7 Hz, corresponding to an inverter propagation delay of 27 ms. To the best of the author's knowledge, this is only the second rail-to-rail organic ring oscillator reported. Compared to state-of-the-art 2.3 ms delay OTFT digital circuits, the logic presented here uses 42 times less area, 10,000x less switching current, and 10x-20x less off-state current [1].

Some of the first OTFT analog circuits are presented. A two-stage, uncompensated operational amplifier was fabricated and characterized. The op-amp used a bias current of 55 pA, had an open loop gain of 36 dB, an input offset of 400 mV, and a unity gain frequency of 7.5 Hz. The dominant poles were due to parasitic overlap capacitances at the outputs of the first and second stages. Only one other operational amplifier has been reported in literature. The design presented here is measured to have a similar gain-bandwidth product while operating at an order of magnitude lower V_{DD}.

A proof-of-concept comparator consisting of a differential amplifier and latch was designed and tested. The comparator was found to have a latch time constant of approximately 32 ms. The comparator was measured to have an input offset of 200 mV. This is the only reported comparator in literature.

These organic circuits demonstrate the possibility of truly low power and flexible electronics for applications where speed is not essential.

5.1 Measurement Setup

Fabricated wafers were tested in nitrogen ambient using a Signatone probe station. Because of the large number of pads required for the circuits, a probe card was used in place of micropositioners to contact the pads. The probe card, obtained from SV Probe, was able to

contact 24 pads simultaneously. These signals were brought to an Agilent 4156C semiconductor parameter analyzer, Tektronix 3102 arbitrary function generator and Hewlett-Packard 4140B picoamp meter/DC voltage source. The probing setup is pictured below.

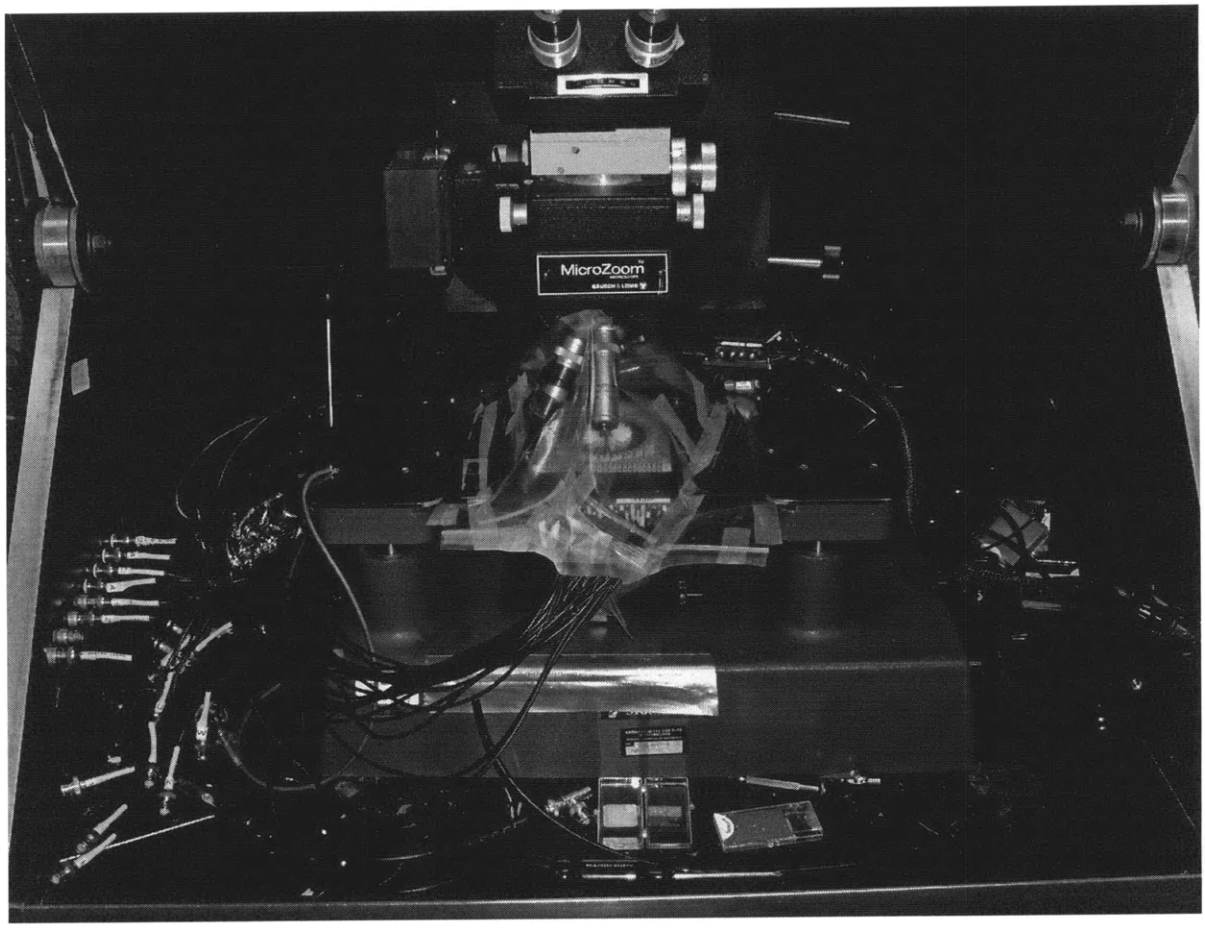


Figure 5-1: Setup showing probe station, probe card, and plastic enclosure for testing in nitrogen ambient.

All circuits discussed in this chapter were tested using this setup.

5.2 Digital Circuits

Described in detail in Chapter 3, the inverter is the basic building block for digital systems. The dual V_T inverters presented here were designed to maximize noise margins, and minimize area. Two inverter topologies were designed – one optimized for a low V_{DD} (3 V), and the other for a higher V_{DD} (5 V). Figure 5-2 illustrates the process of area minimization. The driver width is held constant at 20 μm, and the driver length is varied. The zero-V_{GS} load is re-sized at each point to maximize noise margins and keep the trip point V_M at $V_{DD}/2$. The active area is the total semiconductor and overlap area of both transistors.

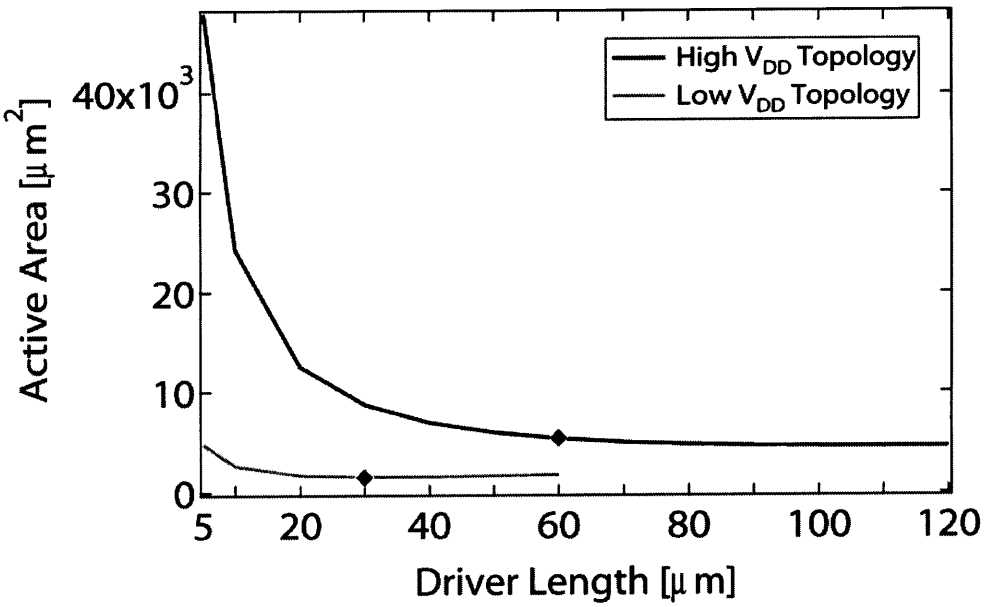


Figure 5-2: Inverter area versus driver length for high and low V_{DD} topologies. Designs chosen are indicated by diamond.

Marked in Figure 5-2, a driver length of 60 μm was chosen for the high V_{DD} topology, and a length of 30 μm was chosen for the low V_{DD} case. The high V_{DD} inverter was used as the common source stage in the operational amplifier and comparator, which will be discussed later in the chapter. The high V_{DD} design was used in these circuits because they required more headroom and hence a higher V_{DD} than the digital logic. The low V_{DD} design was implemented separately and in an 11-stage ring oscillator. Its characterization will be presented here.

The inverter's DC characteristics were obtained using the Agilent 4156C semiconductor parameter analyzer. The input voltage was swept from 0 to 3 V with 100 mV steps. The output voltage and supply current from V_{DD} were measured. The transfer characteristics are pictured in Figure 5-3.

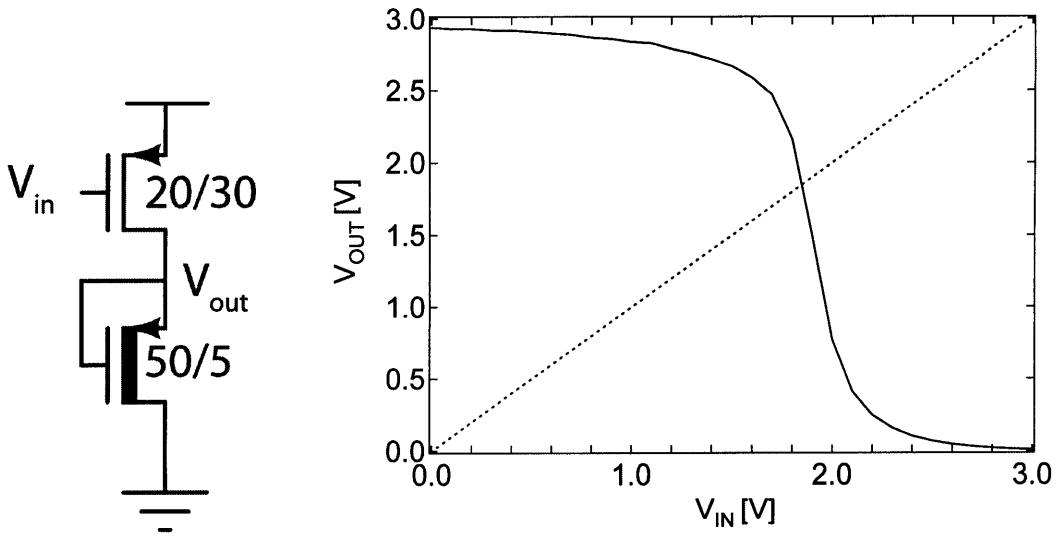


Figure 5-3: Inverter schematic (left). Measured inverter transfer characteristics (right).

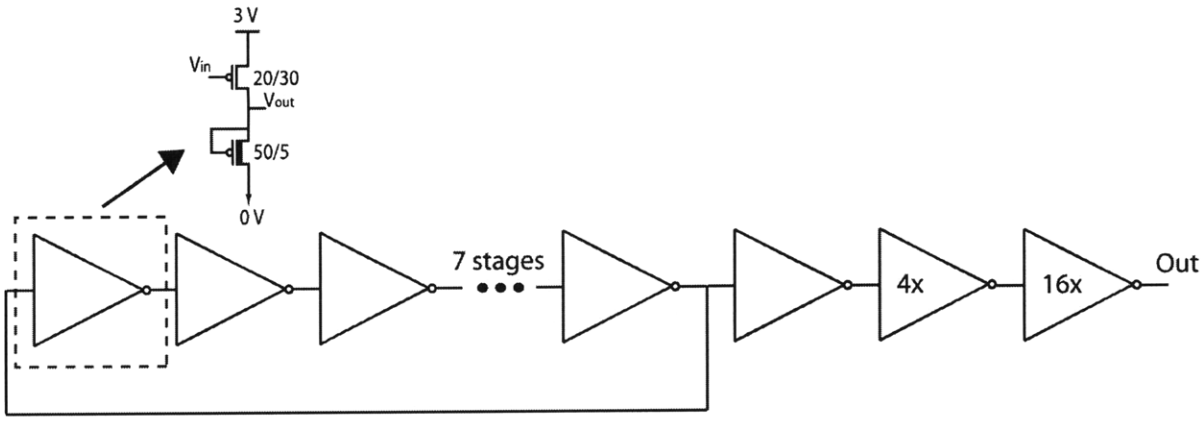
As confirmed by its noise margins, the inverter is functional and sinks 8 pA at its trip point. The inverter was designed to trip at $V_{DD}/2$, but trips at ~1.8 V, since the Pt gate device V_T was slightly more negative than was used in the hand designs. An explanation of noise margins can be found in Chapter 3. The table below summarizes the performance of the inverter.

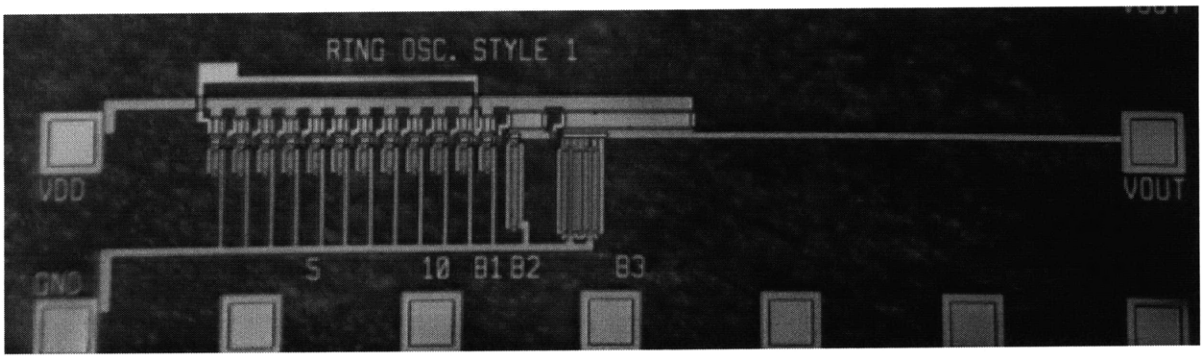
Metric	Value
Noise Margin High	0.29 V
Noise Margin Low	1.4 V
Trip Point	1.8 V
Voltage Gain at Trip Point	-7 V/V
Current at Trip Point	8 pA
Off Current ($V_{IN}=V_{DD}$, $V_{IN}=0V$)	480 fA, 9 pA
V_{DD}	3 V

Table 5-1: Performance summary of low V_{DD} dual V_T inverter.

An 11-stage ring oscillator was implemented using the low V_{DD} topology. The ring oscillator has two main purposes – it can be used to generate a clock signal on chip, and its oscillation frequency indicates the inverter propagation delay. A three-stage output buffer was implemented to enable the ring oscillator to be probed without loading it and changing its oscillation frequency. The schematic of the ring oscillator is pictured in Figure 5- 4.

The 11-stage ring oscillator was tested by applying V_{DD} and ground and measuring the output transient at the output of the buffer. The initial start-up transient is not pictured.





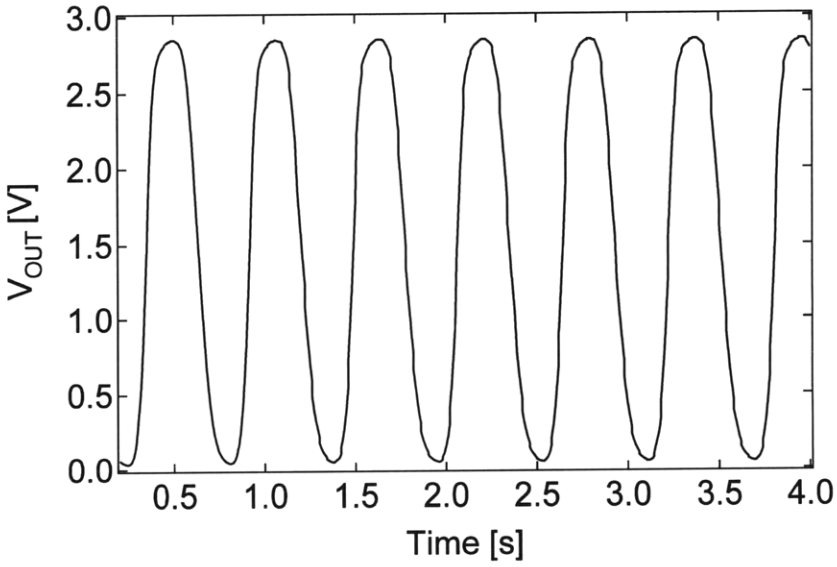


Figure 5-4: 11-stage ring oscillator with output buffer (top). Die photograph of ring oscillator (middle). Measured output transient (bottom).

The ring oscillator was observed to swing near rail-to-rail (2.86 V to 0.05 V), and is only the second reported rail-to-rail organic ring oscillator [1]. The output waveform can also be used to extract the inverter propagation delay. According to *Rabaey and Chandrakasan*, the inverter propagation delay of this 11-stage oscillator is $1/22^{nd}$ the oscillator period [2]. For this ring oscillator, the period is 588 ms, corresponding to an inverter propagation delay of 27 ms.

The inverter and ring oscillator described here are some of the few functional OTFT digital circuits published in literature. The power consumption and power supply used are both record lows for integrated OTFT circuits [1,3,4].

The table below compares these results to state-of-the-art integrated organic digital circuits. Unfortunately, not all performance specifications are reported in literature. Although other papers have quoted inverter propagation delays, to the best of the author's knowledge only *Klauk et al.* have demonstrated a rail-to-rail ring oscillator from which to extract the delay. A non rail-to-rail ring oscillator does not give a representative value for the actual inverter delay. *Klauk* demonstrates organic circuits at a power supply of 1.5 V, but only his results using a 3 V supply are shown for comparison.

Author	**Klauk et al. (2007) [1]**	**Cantatore et al. (2007) [4]**	**This work (2009)**
V_{DD}	3 V	30 V	3 V
Inverter topology	CMOS push-pull	PMOS, Zero-V_{GS}	PMOS, Zero-V_{GS}
Technology	Shadow-mask patterned evaporated pentacene and $F_{16}CuPc$ (n-type)	Photolithographically patterned spin-cast pentacene	Photolithgraphically patterned dual V_T evaporated pentacene
Active-Area	66000 μm^2	Unreported (L=4 μm)	1550 μm^2
Noise Margins	NM_H=1.3 V, NM_L=1.3 V (both estimated)	2.04 V (reported as sum)	NM_H=0.29 V, NM_L=1.4 V
Static Current	10 pA ($V_{IN}=V_{DD}$), 100 pA (V_{IN}=0V)	Unreported	480 fA ($V_{IN}=V_{DD}$), 9 pA (V_{IN}=0V)
Switching Current	~100 nA	Unreported	8 pA
Inverter Propagation Delay	2.3 ms	Unreported	27 ms
Power-Delay Product	$2.3x10^{-10}$ J	Unreported	$2.2x10^{-13}$ J

Table 5-2: Performance comparison between state-of-the-art organic digital circuits.

The noise margins of the dual V_T inverters are significantly better than those of *Cantatore et al.* The noise margins measured here comprise 56% of V_{DD} compared to *Cantatore's* 7% of V_{DD}.

These inverters offer tremendous power and area savings compared to the work of *Klauk.* The dual V_T inverter occupies 42x less area, uses 10,000x less switching current, and 10x-20x less static current (V_{IN}=0 V, V_{IN}=V_{DD}, respectively). The main reason for the large (10^3) power-delay product improvement is largely due to the significantly smaller channel length and overlap capacitance in this work. Since *Klauk*'s inverters are fabricated by shadow-masking, the minimum channel length and gate-source/gate-drain overlaps are 20 μm each, significantly increasing the load capacitance of the inverter. The dual V_T inverter demonstrated here was not optimized for speed. If the dual V_T inverter was optimized for speed, the estimated delay would be 3.5x shorter, i.e. 7.7 ms.

The measured inverter characteristics also indicate that a complementary process is not necessary to have positive noise margins and low power. In fact, integrating a complementary device is only clearly advantageous if the mobility of both devices are comparable. Assuming devices have symmetric V_T's, if the p-channel's μ_h equals the μ_e of the n-channel device, then both devices should have the same W/L to make the inverter trip at $V_{DD}/2$. If μ_h= 10*μ_e, then the n-channel device will need a 10x larger W/L. Therefore, we see that a poor mobility device will need to be sized much wider and therefore dominates the load capacitance.

The dual V_T inverter's load is 15x larger than the driver. This implies that an n-channel device's electron mobility would need to be at least $1/15^{th}$ the hole mobility of pentacene to offer any real benefit. *Klauk* uses an n-channel semiconductor with $1/30^{th}$ the mobility of pentacene, but only sizes the n-channel device 10x wider. This is because the p-channel and n-channel devices V_T's are asymmetric – the n-channel device is more depletion-mode than the pentacene device.

5.3 Analog Circuits

5.3.1 Differential Pair

The differential amplifier is an analog circuit that amplifies the difference between two input voltage signals. It is commonly used as the first stage for operational amplifiers and comparators.

The standard MOS differential pair topology consists of a tail current source, connected to the source of two common source amplifiers. The input signals are connected to the gates of common source drivers, and the outputs are taken at the drains of these devices. A schematic of this topology is illustrated in Figure 5-5. If all devices are perfectly matched, and the

voltage inputs are equal, then the current from the current source will be evenly split between both branches and the differential pair's outputs will be at the same voltage. If one input becomes higher than the other, the overdrive of that transistor will decrease, and as a result the current through that branch will lower, thereby decreasing the output voltage at that branch's output.

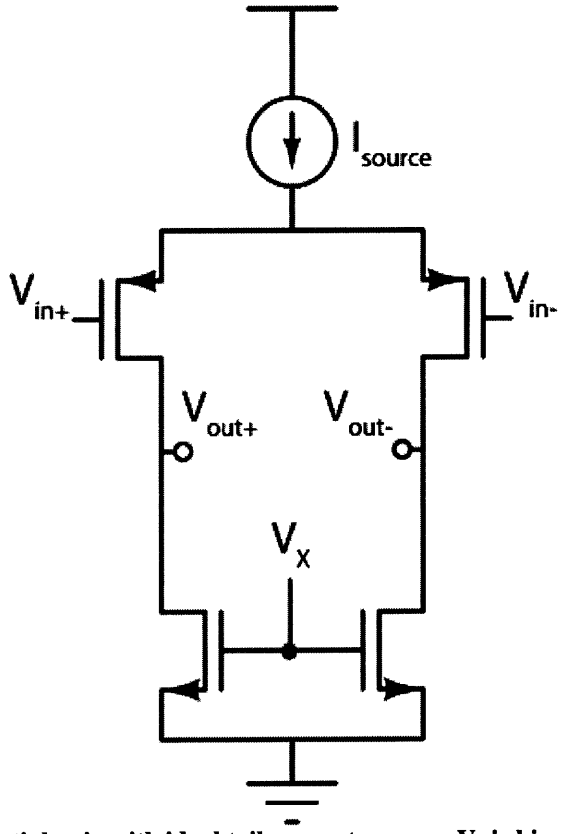


Figure 5-5: MOS differential pair with ideal tail current source. V_x is biased by an external voltage source.

In the dual V_T OTFT technology, the MOS differential pair is implemented with zero-V_{GS} loads, and a current mirror in place of the ideal source, shown in Figure 5-6. The current source in the mirror is supplied by the 4156C parameter analyzer.

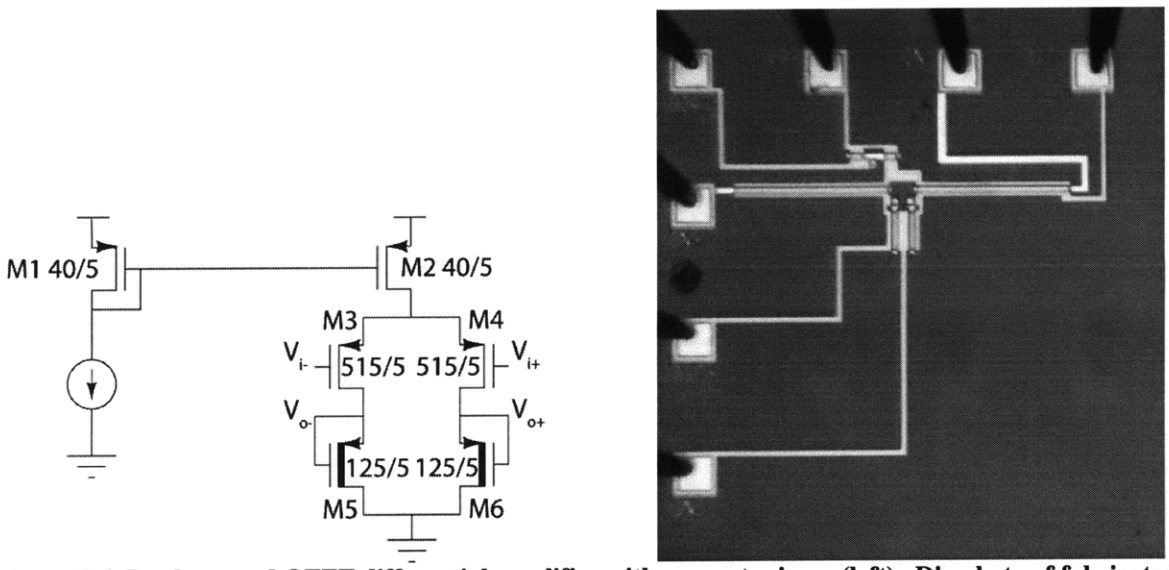


Figure 5-6: Implemented OTFT differential amplifier with current mirror (left). Die photo of fabricated differential amplifier (right).

Performing the small signal analysis for the circuit in Figure 5-6, one finds that the ideal differential pair will have a differential voltage gain given by Equation 5-1. In the OTFT implementation, devices were sized to have the output centered at $V_{DD}/2$ when the inputs were at a common mode of $V_{DD}/2$. The circuit was designed for a differential gain of -30 V/V.

$$A_{v,diffrential} = -g_{m,input} * \left(r_{o,load} \parallel r_{o,driver}\right) \tag{5-1}$$

The differential amplifier was fabricated, and tested with the 4156C parameter analyzer. The output voltages of the differential pair were measured by the 4156C while the differential input voltage was swept point-by-point at a given common-mode bias. Two common mode voltages were tested, 2.4 V and 3.4 V. The differential input voltage range for each common mode bias is different, since the maximum voltage applied, $V_{CM} + V_{differential}$, is limited to 5 V. For example, the differential input voltage can go to 2.6 V for V_{CM}=2.4 V, but only 1.6 V for V_{CM}=3.4 V. The measured results are plotted in Figure 5-7 and indicate an input offset of 200 mV. The differential gain is 23.5 dB at V_{CM}=3.4 V.

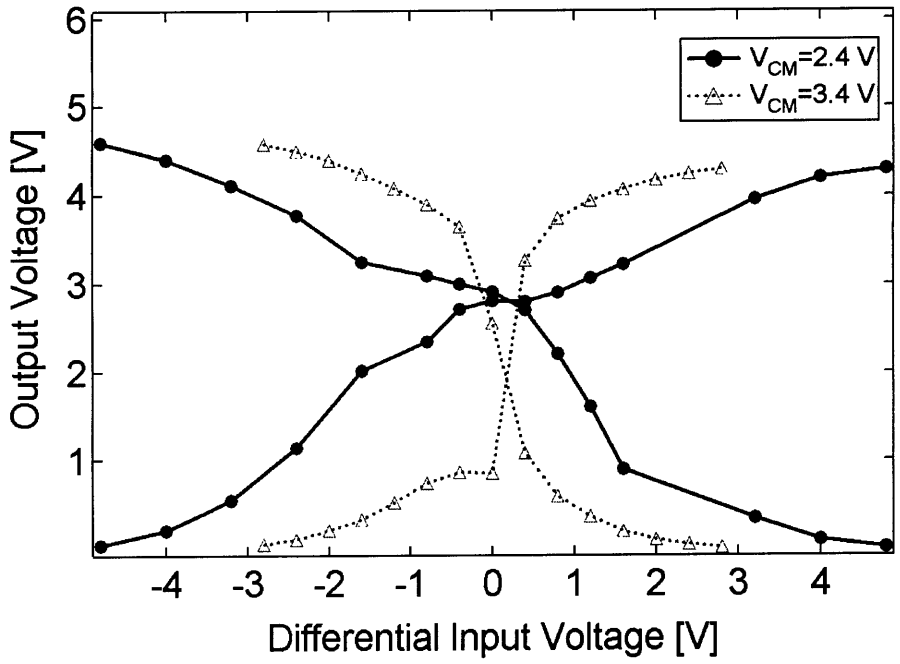


Figure 5-7: Output voltage versus differential input voltage for V_{CM}= 2.4 V, 3.4 V. At V_{CM}=3.4 V, the differential gain is 23.5 dB and the input offset is 200 mV.

At high common mode input, the drain voltage of the current source moves high, making it go into triode. This lowers the current through the differential pair, putting the zero-V_{GS} loads into the triode region. At low common mode inputs, here 2.4 V, the input pair goes into triode, since the zero-V_{GS} loads must have enough V_{DS} across them to support the current through each branch.

We can also find the common-mode gain by looking at the change in the output voltages as the inputs are changed together. From Figure 5-7, we see that the common mode gain is ~ 1. The common-mode rejection ratio (CMRR) is defined as follows:

$$CMRR = \frac{A_{v,differential}}{A_{v,common-mode}} \tag{5-2}$$

The CMRR of this differential amplifier is 23.5 dB.

This is the highest gain differential pair reported in the literature. There are only two other differential pairs published. Their results and these are compared below.

Author	Kane et al. [3]	Gay et al. [5]	This work
Technology	PMOS photolithographic evaporated pentacene	PMOS photolithographic evaporated pentacene	PMOS photolithographic dual V_T evaporated pentacene
Load	Diode-connected	Diode-connected	Zero-V_{GS}
Gain	18.6 dB	10 dB	23.5 dB
Input Offset	600 mV	Unreported	200 mV
V_{DD}	30 V	40 V	5 V
Power	Unreported	Unreported	300 pW

Table 5-3: Performance comparison between state-of-the-art organic differential amplifiers.

All other reported differential pairs in the literature use a diode-connected load. Therefore, it is no surprise that this implementation offers significantly higher gain - two times the previous best. Additionally, this design has the lowest input offset and V_{DD} reported.

5.3.2 Effect of Mismatch and Input Offset in the Differential Pair

The input offset is defined as the voltage difference required between the two inputs in order for the differential pair's outputs to be at the same voltage. Input offset in the differential pair arises from mismatch between the input pair and load devices. Consider the differential pair in Figure 5-8. Following the approach in [6], we take the voltage loop around the input pair. Let $V_{offset}=V_{i-}-V_{i+}$. We can write the voltages around the loop as:

$$V_{offset} - V_{SG3} + V_{SG4} = 0 \tag{5-3}$$

If all devices are perfectly matched then when $V_{i-}=V_{i+}$, the currents through both branches are equal ($I_1=I_2$), and $V_{o-}=V_{o+}$. V_{offset} therefore equals 0 V.

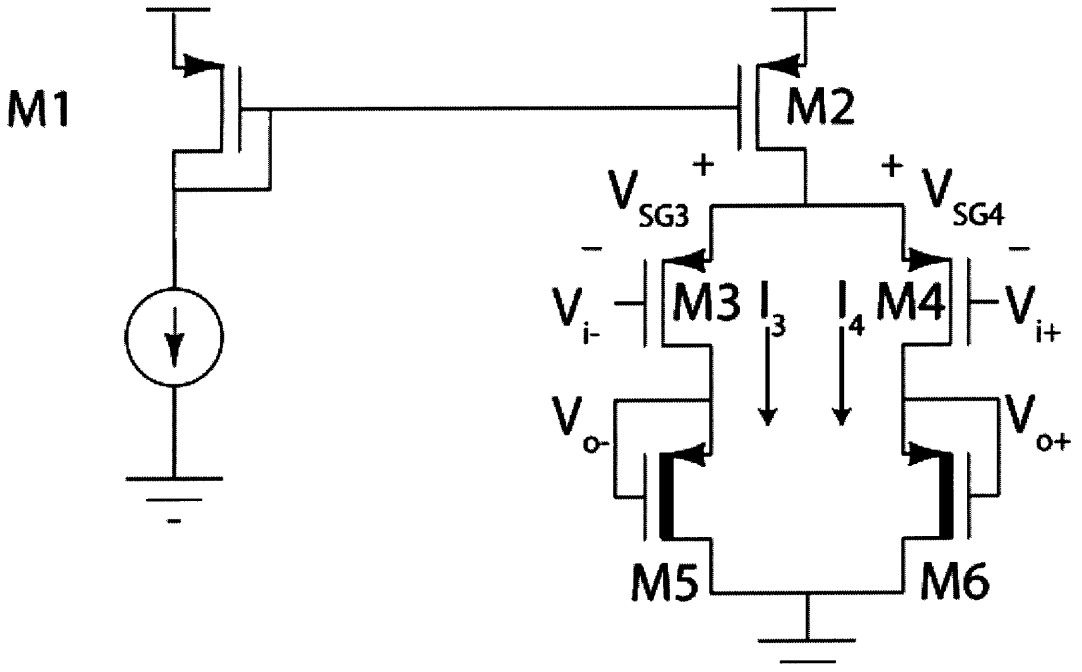


Figure 5-8: Differential amplifier for determination of mismatch.

Assuming M3 and M4 are in saturation, the V_{SG}'s of M3 and M4 can be replaced with terms from the drain current Equation 1-6. Re-writing Equation 5-3 yields

$$V_{offset} = V_{SG3} - V_{SG4} = \Delta V_T + \sqrt{\frac{2I_{SD3}}{K_3}} - \sqrt{\frac{2I_{SD4}}{K_4}} \tag{5-4}$$

where $K = \mu \frac{W}{L} C_{ox}$. This equation reveals the relationship between the offset and circuit design parameters. By re-arranging and making the approximation that $\sqrt{x} \approx \frac{1+x}{2}$ we arrive at Equation 5-5 [6].

$$V_{offset} \approx \Delta V_{T3-4} + \Delta V_{T5-6}\left(\frac{g_{m5,6}}{g_{m3,4}}\right) + \frac{(V_{SG}+V_t)_{3,4}}{2}\left(\frac{-\Delta(W/L)_{3,4}}{(W/L)_{3,4}} - \frac{\Delta(W/L)_{5,6}}{(W/L)_{5,6}}\right) \tag{5-5}$$

Equation 5-5 indicates that any mismatch between the input pair's threshold voltages will result in a linear increase in the differential amplifier's input offset. Mismatch in the zero-V_{GS} loads' V_T's will be multiplied by the ratio of the input pair g_m to the load g_m. To minimize this term's contribution, one should size the input pair much wider than the load. In this implementation of the differential pair, the ratio of g_m's is 0.05, meaning that the load

V_T mismatch will be attenuated by 20x. The third term is proportional to the overdrive of the input pair divided by two. For this differential pair, the overdrive is ~ 1.9 V. To reduce input offset, one would want to decrease the overdrive. It is important to note that the three quantities in Equation 5-5 do not necessarily add constructively. Each device parameter in Equation 5-5 has its own distribution, whose mean should be 0.

The standard deviation of the threshold voltage for both Al and Pt devices was measured to be approximately 100 mV. Therefore, a ΔV_T of $\pm 1\sigma$ is 200 mV. Although un-measured, we assume a W/L mismatch of 2%. With these assumptions, Equation 5-5 is evaluates to 230 mV. The measured input offset is 200 mV.

5.3.3 Clocked Comparator

A comparator is an analog circuit block that takes two analog voltage inputs, V_{in1} and V_{in2}, and outputs a digital voltage depending on the difference between V_{in1} and V_{in2}. For a comparator with power supply V_{DD}, an ideal comparator implements the following function.

$$\begin{aligned} V_{in2} < V_{in1} &\rightarrow V_{out} = V_{DD} \\ V_{in2} > V_{in1} &\rightarrow V_{out} = 0 \end{aligned} \tag{5-6}$$

An ideal comparator has infinite gain, and produces a digital "zero" or "one" for any value of V_{in2}-V_{in1}. A graphical representation of an ideal comparator and its transfer characteristics are shown below.

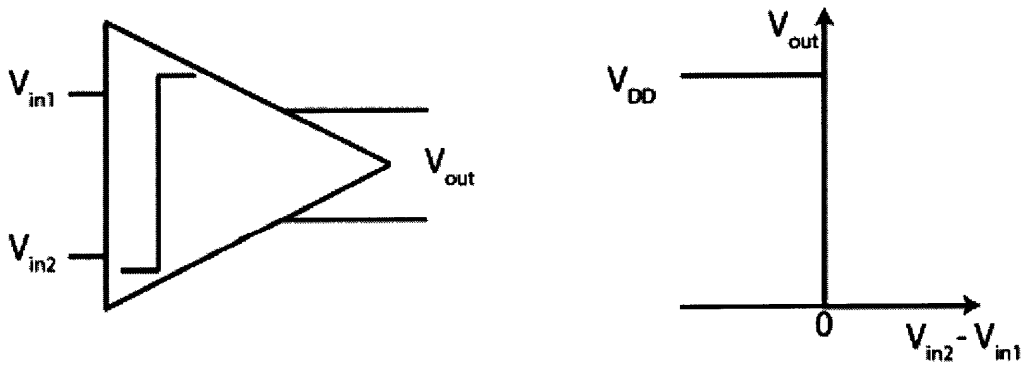


Figure 5-9: Ideal comparator and DC voltage transfer characteristics.

The comparator is a fundamental building block for most analog-to-digital converters (ADCs). In an organic sensing system, such as the one described in Chapter 2, an integrated ADC would be necessary to take in the analog signals, convert them to the digital domain, and send them off the substrate. This approach would be preferred to sending the analog signals immediately off the organic substrate to silicon, as digital signals would be less susceptible to noise encountered during routing.

One of the simplest ADC designs is a flash architecture. This topology consists of 2^N -1 comparators for an N-bit ADC. A resistor ladder consisting of 2N resistors creates reference voltages at the nodes connecting each resistor. Each resistor has a voltage drop equal to 1 least significant bit (LSB) greater than that of the resistor below it. These reference voltages are inputted to a comparator, whose other input is the signal we wish to digitize, V_{in}. All comparators for which $V_{in} > V_{ref}$ will output a logic "1" , and those for which $V_{in} < V_{ref}$ will output a "0", creating a "thermometer code". This thermometer code is not a binary representation of the input signal, and must be converted to binary through a decoder circuit. The circuit schematic of a 3-bit flash ADC is shown here.

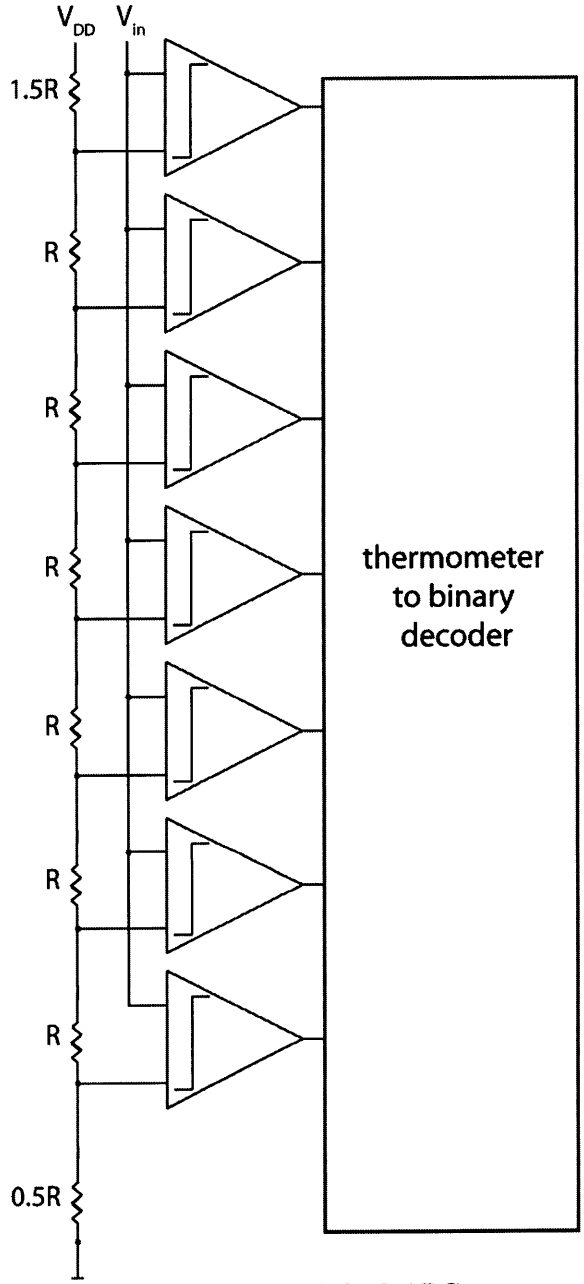


Figure 5-10: 3-bit flash ADC

There are a number of ways to implement a comparator circuit – any amplifier with high gain would work. However, simply using a high gain amplifier is not the best choice. The amplifier's slew can be approximated as a current source charging a capacitor. Therefore, to achieve a fast comparator, a linear increase in current achieves a corresponding increase in speed.

A simple amplifier is not the best choice for a comparator - since there is no need for stability in a comparator, positive feedback can be used. Using a latch, i.e. two cross-coupled inverters, we will show that the output voltage increases exponentially with time. With positive feedback, a much faster topology that doesn't trade off linearly with power can be obtained. Shown below are two identical inverters connected in positive feedback.

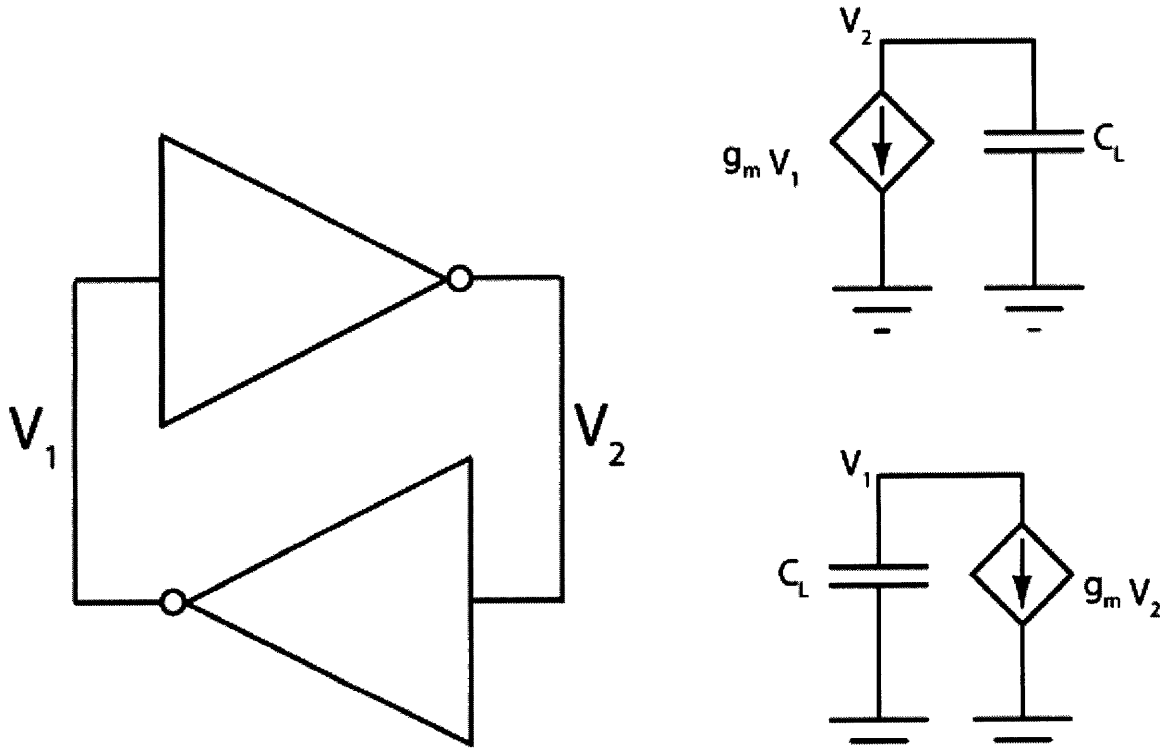


Figure 5-11: Latch with two initial voltages, V_1 and V_2, and linearized model. After [7].

At the two inputs to the latch are initial voltages V_1 and V_2. We assume the inverters are in the linear, high gain regime, and model them as voltage-controlled current sources driving a load, C_L [6,7]. The characteristic equation is given in Equation 5-7, where g_m is the transconductance of the inverter driver, and C_L is the capacitance at node V_1 and V_2.

$$g_m V_1 - g_m V_2 = -C_L \frac{dV_2}{dt} + C_L \frac{dV_1}{dt} \tag{5-7}$$

By noting $\Delta V=V_1-V_2$, we can re-write the equation.

$$\frac{d\Delta V}{dt}=\frac{g_m}{C_L}\Delta V \tag{5-8}$$

The solution to this first-order differential equation is shown below, where ΔV_O is the initial voltage difference between V_1 and V_2.

$$\Delta V=\Delta V_o e^{t/\tau} \tag{5-9}$$

Since the exponent is positive, the ΔV will increase exponentially with time. The time constant for the ideal latch is given in Equation 5-10.

$$\tau=\frac{C_L}{g_m} \tag{5-10}$$

The output voltages of the latch will exponentially tend towards the voltage rails, as shown in the Figure 5-12.

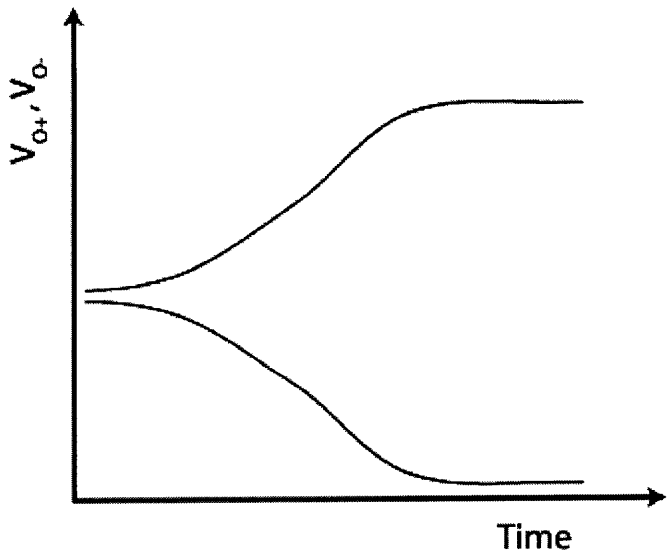


Figure 5-12: Illustration of latch behavior versus time.

Although one could use only a latch as a comparator, a preamplifier cascaded with the latch is preferred. This architecture allows the difference between the two inputted signals to be amplified before sending it to the latch. Equation 5-9 tells us that increasing ΔV_o will decrease the time required to reach the required ΔV. More importantly, amplification of the input difference is necessary to overcome any offset in the latch. This point will be discussed

in detail further in the section. Lastly, offset cancellation techniques can be more easily used at the amplifier stage to reduce input offsets and enable higher resolution ADCs [8].

The general latch architecture is shown in Figure 5-13. In this design, there are two clock signals, CLK1 and CLK2.

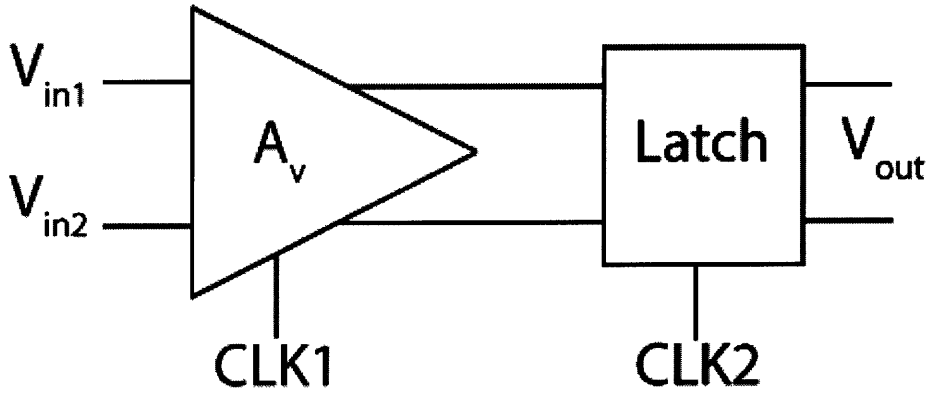


Figure 5-13: Comparator block diagram, with preamplifier of gain A_v, and latch.

The clock signals are required to turn on and off each stage. During phase 1, CLK1 enables the preamplifier and disables the latch, allowing the first stage to amplify the input difference. When this is done, the amplifier turns off, and CLK2 turns on the latch. The amplified difference between V_{in1} and V_{in2} drives V_{out} to either V_{DD} or ground, according to Equation 5-9.

Based on the previous description, one would think that CLK1 and CLK2 should be 180° out of phase. However, depending on the topology, both stages may need to be on for a period of time to enable to the amplifier to charge the input nodes of the latch. When this is done, the latch takes the amplified difference between V_{in1} and V_{in2} , and positive feedback forces the outputs of the latch to V_{DD} and ground, according to the polarity of the input.

A transistor level schematic of the implemented comparator is pictured below. The 22 transistor circuit is one of the most complicated OTFT circuits reported in literature.

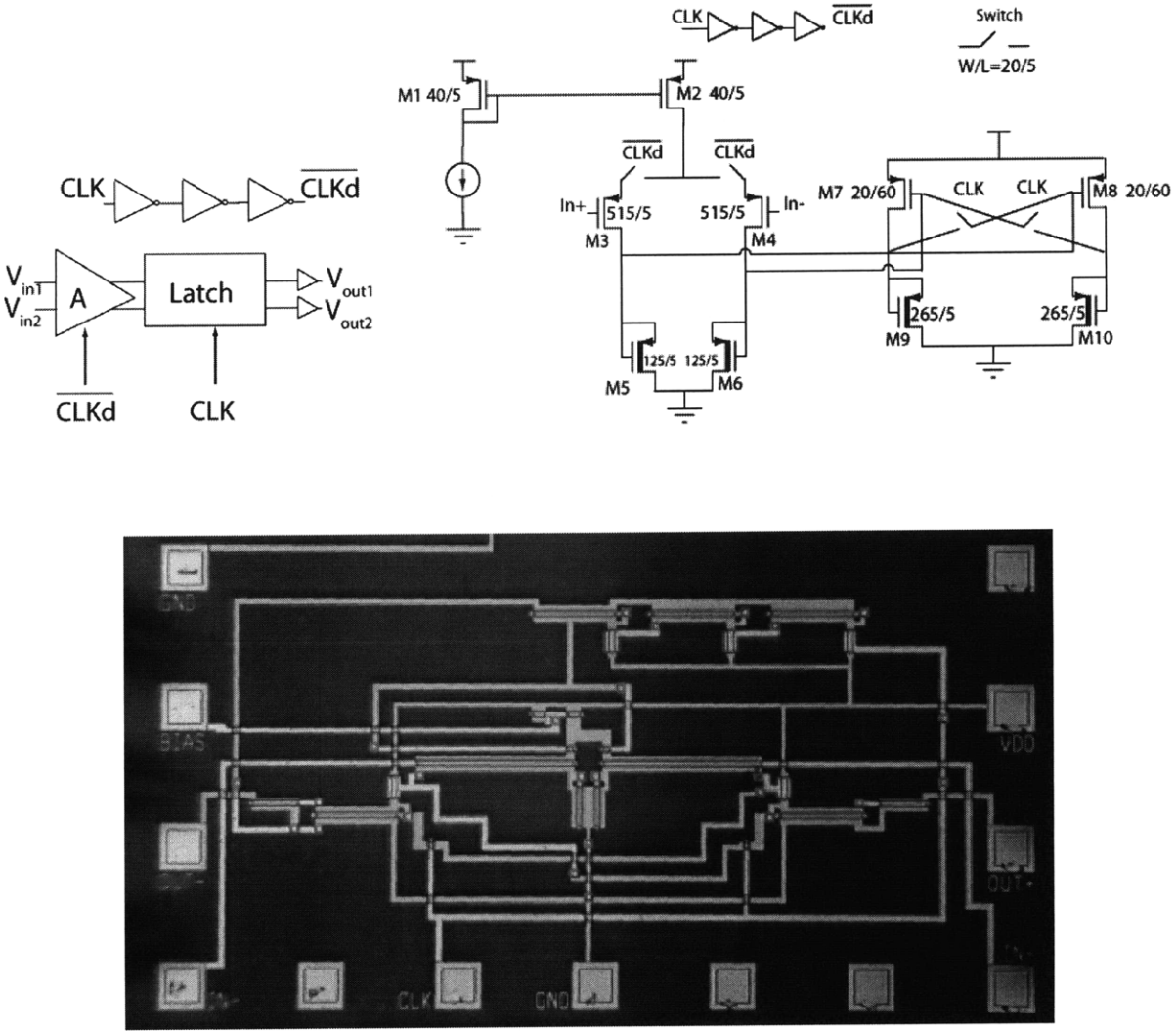


Figure 5-14: Comparator block diagram, with preamplifier of gain A_v, and latch. The buffers at the outputs of the latch are not shown (top). Fabricated comparator die photograph (bottom).

The standard differential pair described earlier was used as the first stage. The standard 5 V, minimum area inverter topology was used in the latch.

Three inverters were used to delay the CLK signal. This keeps the first and second stage on together for 3 inverter delays, between the amplification phase, and latch phase. The inverter design was the same used in the latch.

Figure 5-15 illustrates the clock waveforms. In the first phase, when the amplifier is on and the latch is off, $\overline{\text{CLKd}}$ must be low (i.e. enabled) long enough to allow the amplifier and inverter outputs to be charged to their final values. The equivalent circuit during phase 1 is pictured in Figure 5-16. Since there is no reset feature in the latch, one must wait for the inverter to charge or discharge its outputs from their initial value (the value from the last

comparator decision) to the new correct value, determined by the input to the differential pair.

During the second phase, both stages are on. The equivalent circuit is pictured in Figure 5-17. In this phase, the differential pair and latch are both driving the outputs of the comparator. This implementation used three inverters to delay $\overline{CLKd}$, therefore both stages are on for three inverter delays. Only one inverter delay is necessary to delay $\overline{CLKd}$, because the amplifier is always being loaded by the latch and therefore does not require more time to charge up the latches inputs. If one inverter was used instead of three, the comparator could be clocked at a higher frequency.

In phase 3, the latch drives the outputs to V_{DD} and ground, depending on the polarity of the input. The circuit is shown in Figure 5-18. The clock period must be sufficiently long to allow the latch to reach the require voltage level. The constraints on the clocking frequency previously described are shown mathematically in Equation 5-11.

$$\frac{1}{2f_{clock}} = t_{clock} \geq inverter\ \ delay + t_{differentialpair}$$
$$\frac{1}{2f_{clock}} = t_{clock} \geq inverter\ \ delay + t_{latch} \qquad (5\text{-}11)$$

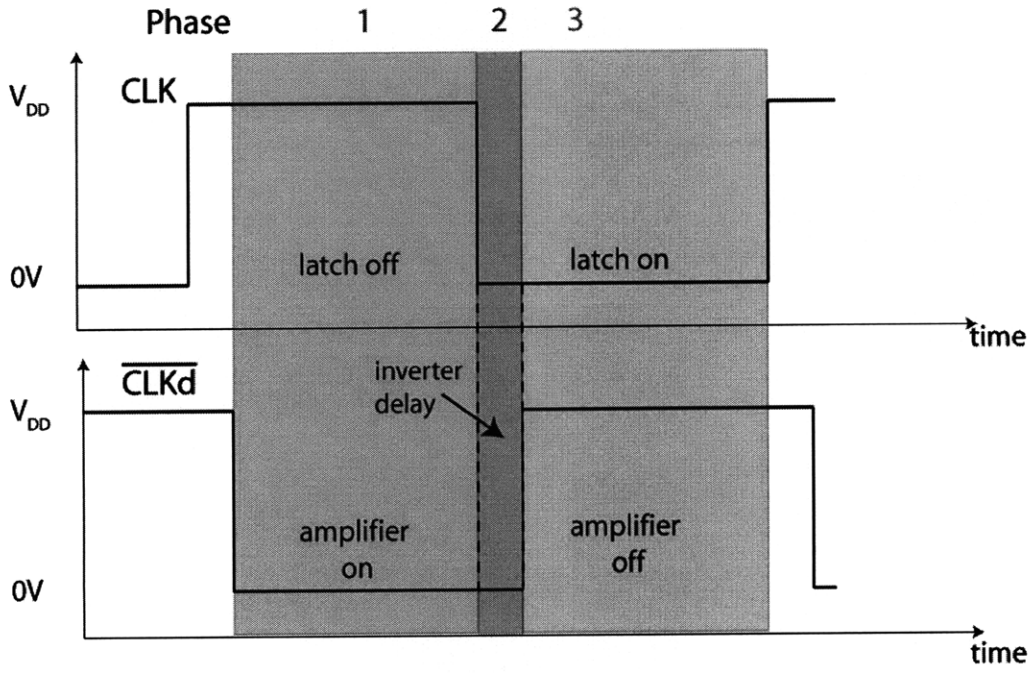


Figure 5-15: Clock signals for comparator.

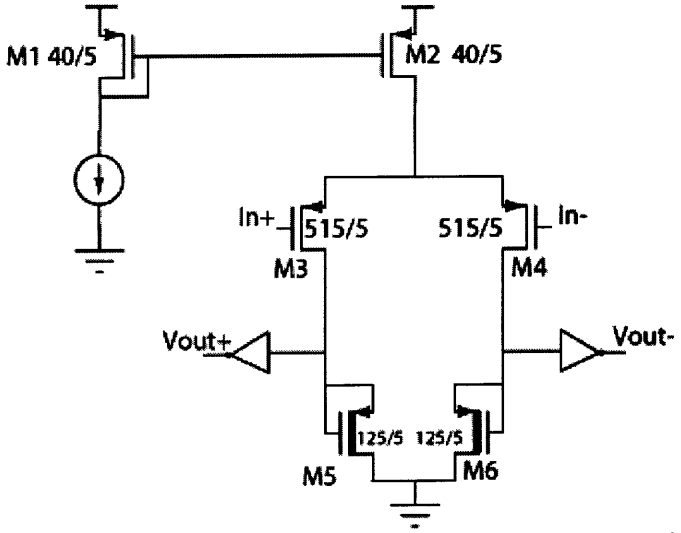


Figure 5-16: Comparator circuit diagram for phase 1, i.e. differential pair on, latch off.

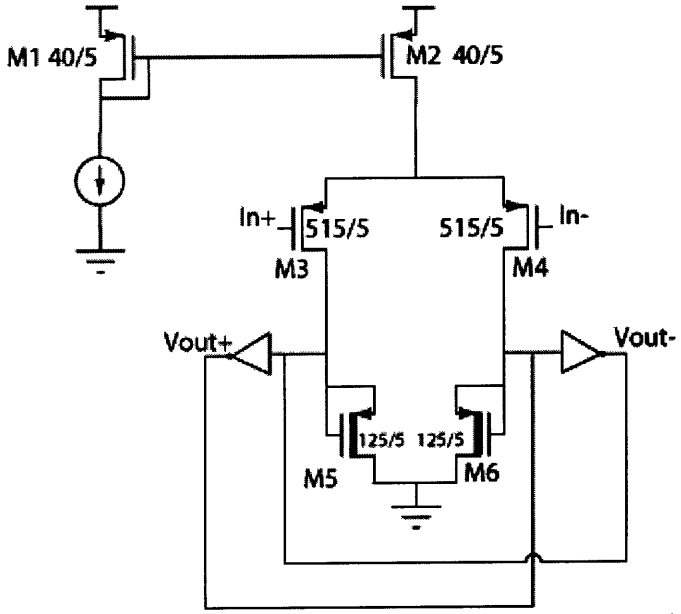


Figure 5-17: Comparator circuit diagram for phase 2 when both clocks are low, i.e. differential pair on, latch on.

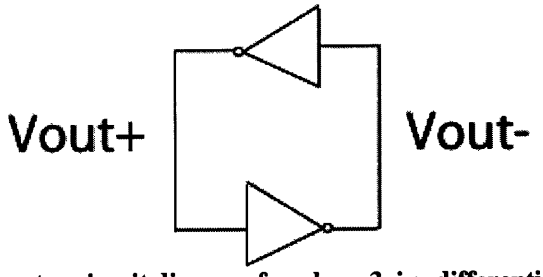


Figure 5-18: Comparator circuit diagram for phase 3, i.e. differential pair off, latch on.

5.3.4 Comparator Transient Measurements

The comparator was measured by applying a 0-5 V square wave clock signal by a Tektronix AFG. A 4156C parameter analyzer was used to source a current which was mirrored to the differential pair. The 4156C also sourced current to the two source followers whose gates were connected to the output nodes of the latch. The 4156C biased the gates of the differential pair's inputs. The comparator output voltages are measured at the output of the inverters, as shown in Figure 5-16. Shown in Figure 5-19 is the transient response measured when both inputs are 3.4 V. Although both inputs are equal, the presence of an input offset will cause the comparator to trip in the direction of the offset.

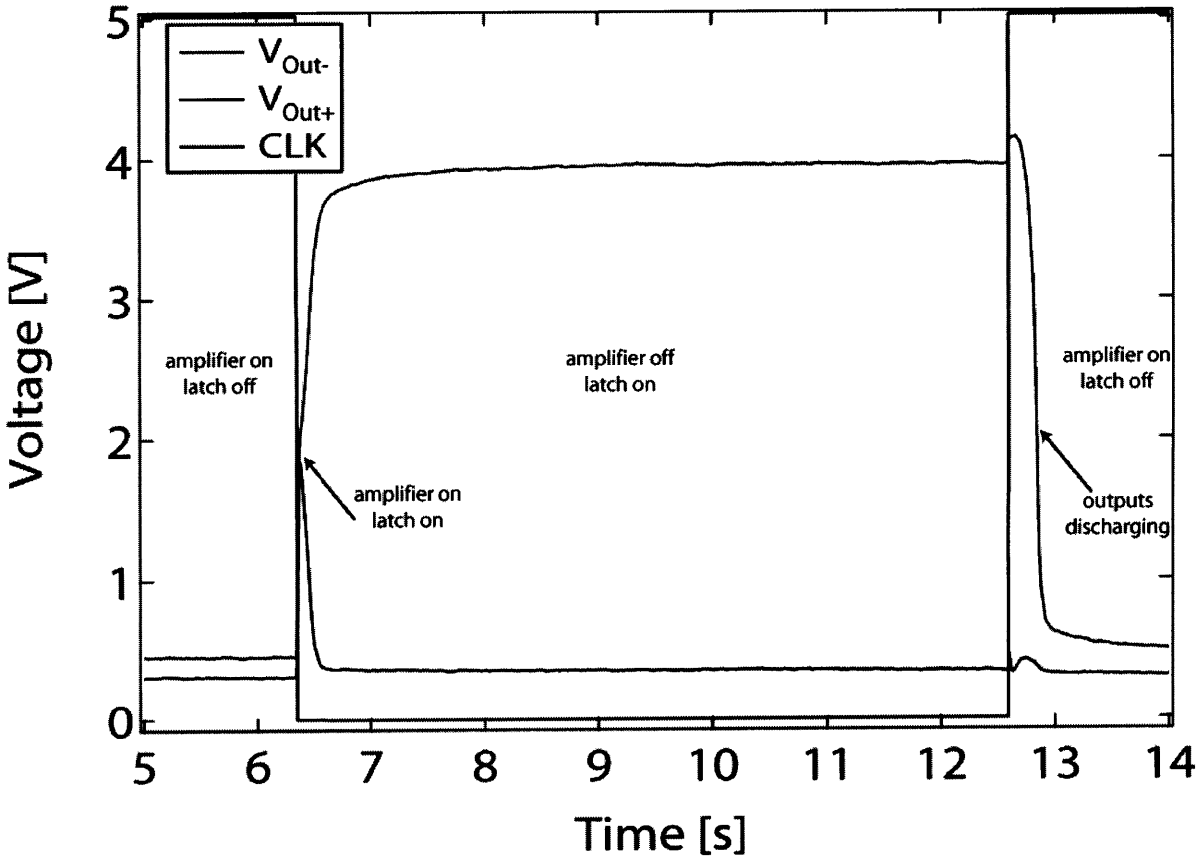


Figure 5-19: Measured comparator output voltage when V_{in+}= V_{in-} = 3.4 V.

This transient depicts the operation described in the previous section. Starting at time= 5 s, the comparator is in phase one (amplifier on, latch off), and one sees that the differential pair has driven the outputs of the inverters to their steady-state DC values. Since there is no reset function, one must wait sufficiently long enough so that the inverters can reach their final

values. Here, it takes 1.53 seconds to reach 99% of the final value. This behavior can be seen at time = 12.5 s.

When CLK goes low (time = 6.4 s), the amplifier and latch are on for a short period of time (phase 2). Here, we see the outputs spike. During this time, as seen in Figure 5-17, the differential pair is driving the outputs of the latch. Figure 5-19 shows that at the end of phase 1 the outputs of the inverters are low, indicating that the differential pair's outputs (the inputs to the inverters) are high. When CLK goes low, the outputs of the inverters are now connected to the output of the differential pair, causing the measured output voltages to move higher.

After three inverter delays the differential pair turns off, and we then see the latch outputs are driven to V_{DD} and ground exponentially, as expected (phase 3). Figure 5-20 plots the output voltages on a smaller time scale.

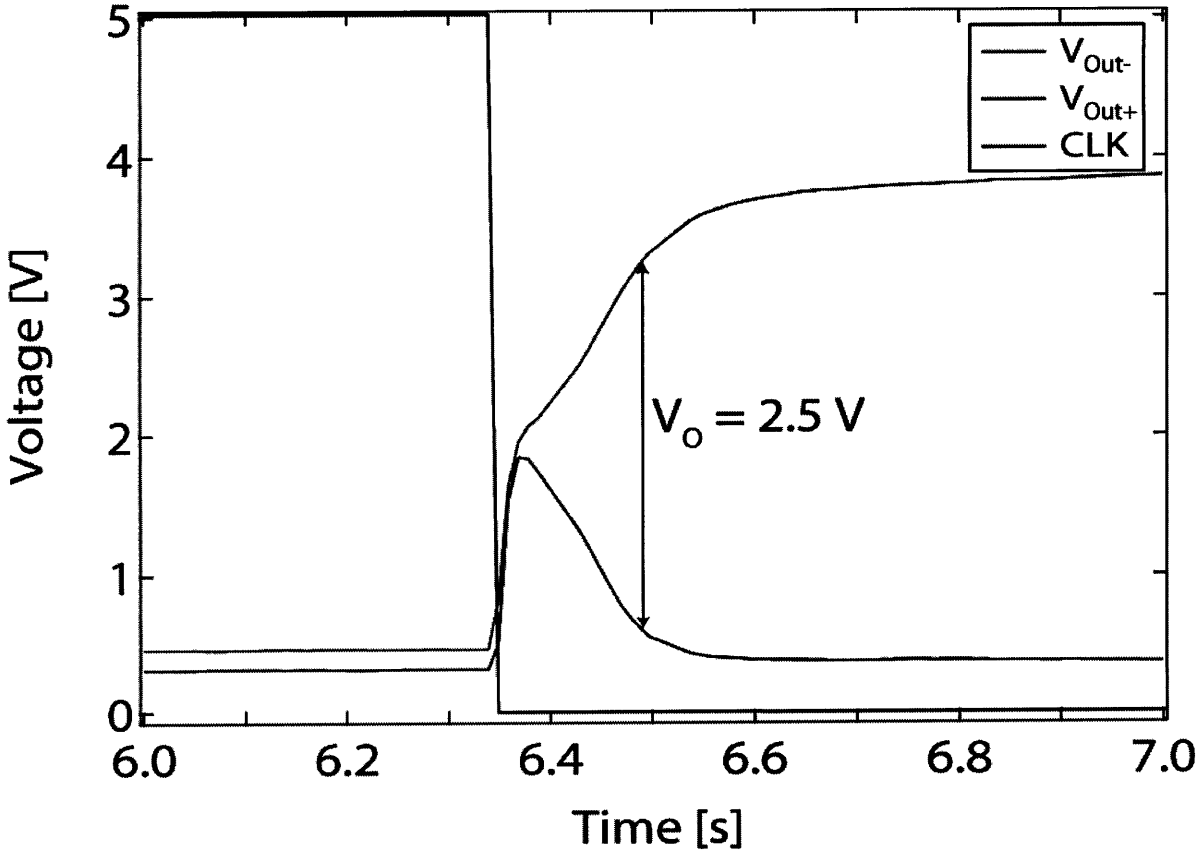


Figure 5-20: Latch outputs versus time. After the latch starts, it takes 119 ms to reach a differential output voltage of 2.5 V.

Figure 5-21 plots the measured comparator output voltages for the case when V_{in+} = 3.2 V, V_{in-} = 3.4 V. Here, we see the comparator now trips with the opposite polarity as before. At

V_{in+}= 3.4 V, V_{in+}= 3.3 V the comparator tripped the other direction, indicating an input offset of ~ 200 mV.

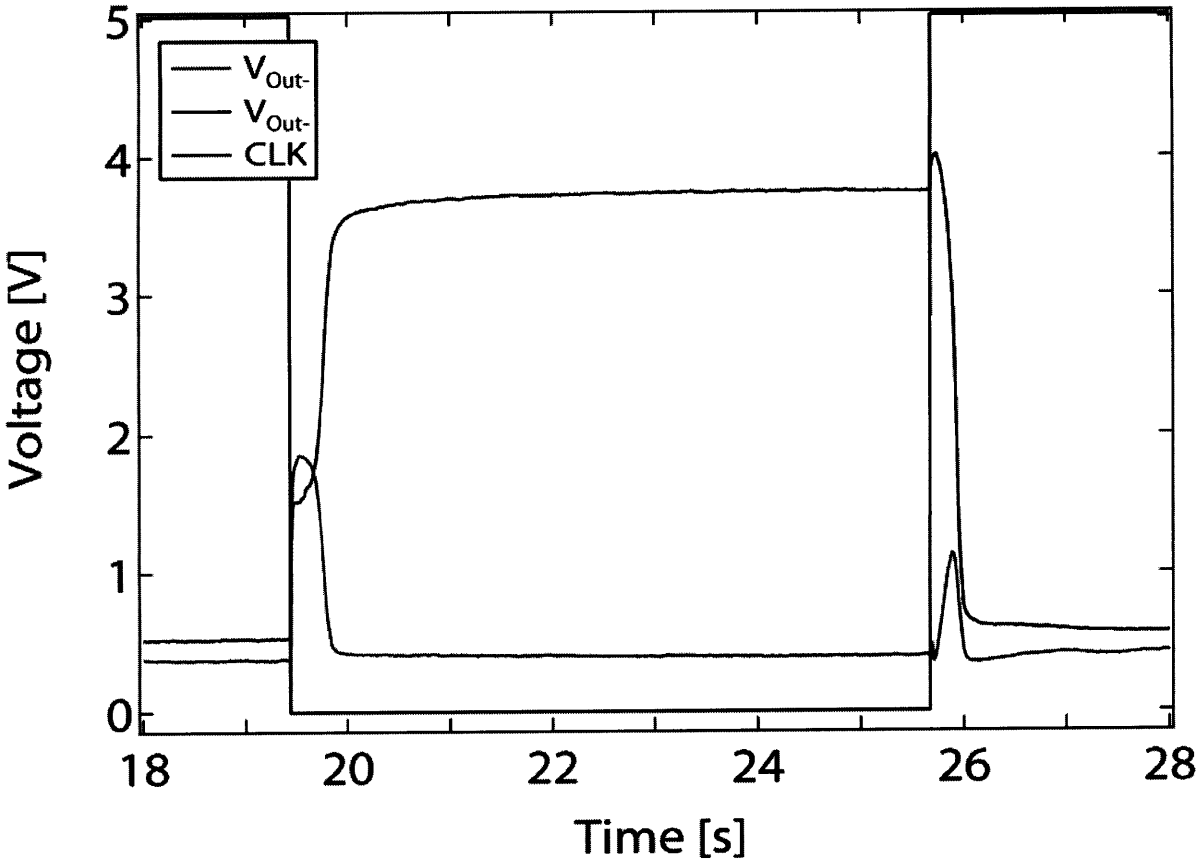


Figure 5-21: Measured comparator output voltage when V_{in+}= 3.2, V_{in-} = 3.4 V.

We now analytically find an expression for the comparator's input offset. In doing so, we must take into account the offset due to the differential pair and any offset in the latch.

The offset in the differential pair was described earlier in the chapter, and found to be:

$$V_{offset} \approx \Delta V_{T,input} + \Delta V_{T,load}\left(\frac{g_{m,load}}{g_{m,input}}\right) + \frac{(V_{SG}+V_t)_{input}}{2}\left(\frac{-\Delta(W/L)_{input}}{(W/L)_{input}} - \frac{\Delta(W/L)_{load}}{(W/L)_{load}}\right) \quad (5\text{-}12)$$

We can find the offset for the latch in the same way as was done for the differential pair. The latch is pictured in Figure 5-22, with switches S1 and S2.

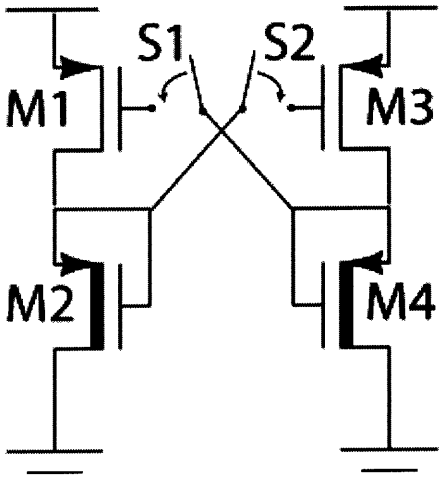


Figure 5-22: Latch with switches S1 & S2. When S1 and S2 are enabled, the inverters become cross-coupled and rail according to the polarity of the input voltage.

The method for finding the offset is as follows [8-10]. We set the outputs of each inverter (the sources of M2 and M4) to be the same voltage. The difference in the gate voltages for M1 and M3 is given by $V_{ID}=V_{SG1}-V_{SG3}$.

Substituting in the drain current from Chapter 1, we can express V_{SG} with the following equation.

$$V_{SG} = -V_T + \sqrt{\frac{2I_{SD}}{K}} \tag{5-13}$$

Using KVL around the inputs to the inverters, we can write the offset, V_{offset}, yielding the same expression as was found for the differential pair.

$$V_{offset} \approx \Delta V_{T1-3} + \Delta V_{T2-4}\left(\frac{g_{m2,4}}{g_{m1,3}}\right) + \frac{(V_{SG}+V_t)_{1,3}}{2}\left(\frac{-\Delta(W/L)_{1,3}}{(W/L)_{1,3}} - \frac{\Delta(W/L)_{2,4}}{(W/L)_{2,4}}\right) \tag{5-14}$$

Switches S1 and S2 control the positive feedback of the latch. When S1 and S2 are disabled, the latch is disconnected. When the input voltage is ready to be applied, S1 and S2 are enabled. Since S1 and S2 are moving from the off-state to the on-state, there is no charge injection from the switches to the capacitance on the output nodes. Any charge injection

would increase the latch offset by the mismatch in charge injected, ΔQ, divided by the node capacitance, C_D. This is a problem for some comparator architectures. However, one still needs to consider the effects of feedthrough. Any mismatch in overlap capacitance between switches S1 and S2, or node capacitances C_D, will result in an extra term, ΔV, in Equation 5-14.

Although the offset in the latch is described similarly as the offset in the differential pair, the ratio of the g_m's of the load and driver are much different. In this case, $g_{m2,4}/g_{m1,3}$ is 4.4. If we use a ΔV_T of $\pm 1\sigma = 200$ mV and 2% W/L mismatch as before, we compute a worst case (i.e. all terms sum constructively) offset in the latch of 1.1 V.

However, the latch offset's contribution to the comparator input offset is attenuated by the gain of the amplifier. In order for the latch to produce the correct output voltages, the differential pair must output a voltage larger than the offset. For example, if the offset of the latch is 1 V, and the preamplifier gain is 10, the latch adds an input referred offset of 100 mV. With these assumptions, we calculate an input offset of 300 mV if all terms add constructively. The input offset for the measured comparator was 200 mV.

$$V_{offset,total} = V_{offset,diffpair} + \frac{V_{offset,latch}}{A_v} \tag{5-15}$$

We can now incorporate the offset term to the latch time, t_{latch}. Rearranging Equation 5-9 and solving for t yields Equation 5-16. Here, C_L is the capacitance at the latch outputs, and is assumed to be the same for both inverters. Using a C_{ox} of 22 nF/cm^2, C_L is calculated to be 1.4 pF. G_m was measured to be ~45 pS for the 20/60 device, giving a C_L/g_m of 0.032 seconds. V_{out} should be $V_{DD}/2$, in this case 2.5 V. We assume that the preamplifier outputs 100 mV more than the latch offset. This yields a t_{latch} of 103 ms. Here, $V_{initial}$ is the voltage output of the differential amplifier.

$$t_{latch} = \frac{C_L}{g_m} \ln\left(\frac{V_{out}}{V_{initial} - V_{offset,latch}}\right) \tag{5-16}$$

Figure 5-20 indicates the latch takes 119 ms to reach a V_{out} of 2.5 V.

There are no comparator results in literature to which to compare. Below, we summarize the dual V_T comparator.

Author	This work (2009)
Technology	Photolithographic dual V_T evaporated pentacene
Load	Zero-V_{GS}
Input Offset	200 mV
Power	5 nW
V_{DD}	5 V

Table 5-4: Performance summary of typical dual V_T OTFT comparator.

5.3.5 Two Stage Uncompensated Operational Amplifier

The operational amplifier is one of the most important analog circuits. The op-amp is used in many applications such as switched-capacitor circuits for filters and analog-to-digital-converters. The op-amp takes two voltage inputs, and outputs one or two voltage outputs, depending on if it is single-ended or fully differential.

An ideal op-amp is shown in Figure 5-23, and has the following characteristics.

1. Infinite input resistance
2. Infinite open-loop gain
3. Infinite bandwidth
4. Zero output resistance
5. Infinite slew rate

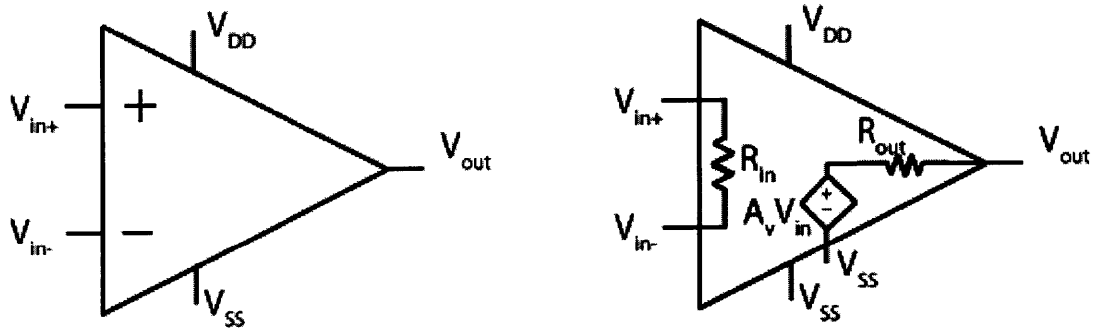


Figure 5-23: Ideal op-amp model (left), and with input and output resistances included (right).

A classic two-stage differential operational amplifier topology was implemented. The first stage is a differential amplifier – the same design described earlier in the chapter. The second stage is a common source amplifier. The minimum active area topology was used. Lastly, a buffer was necessary to probe the outputs of the amplifier with the probe card, which was measured to have a parasitic capacitance of 18 pF. The source follower was designed so that its time constant was ~2 orders of magnitude smaller than the time constants in the amplifier. The circuit is pictured in Figure 5-24.

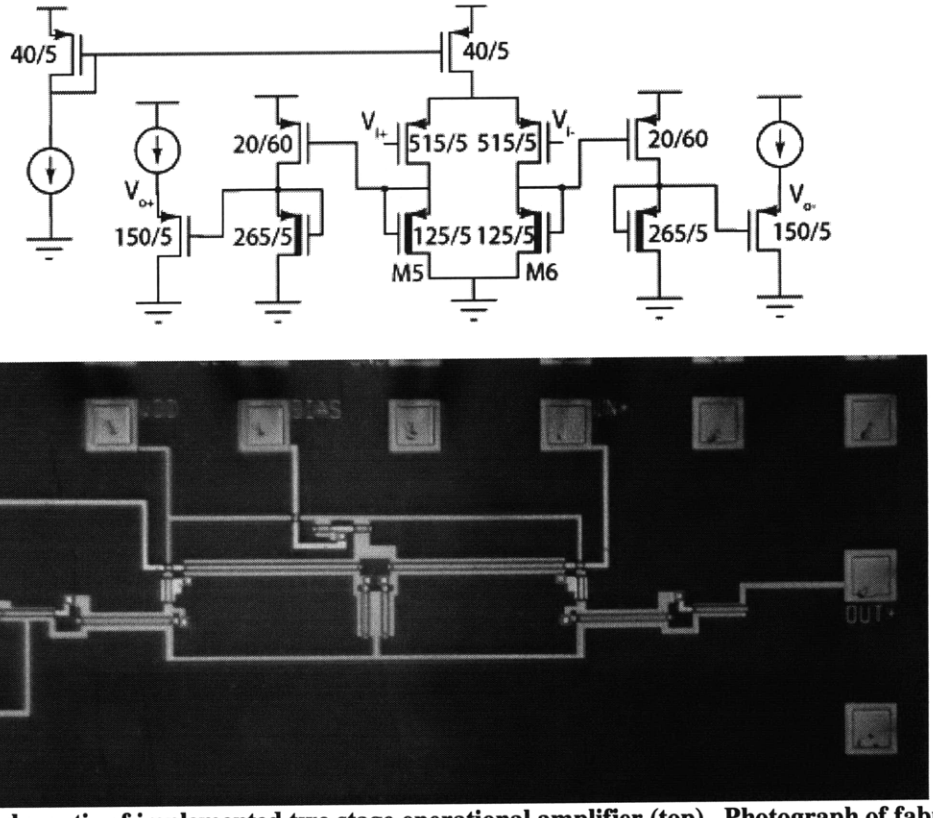


Figure 5-24: Schematic of implemented two stage operational amplifier (top). Photograph of fabricated operational amplifier (bottom).

A number of measurements were done on the operational amplifier to extract performance metrics, perhaps the most important of these being the frequency response.

The open loop frequency response was measured by biasing one input terminal with the 4156C, and applying a DC bias and voltage sinusoid with a Tektronix 3102 Arbitrary Function Generator. The DC bias was equal to the other terminals DC bias + input offset. The output was measured for a given input frequency, and the gain extracted. The input was then incremented to a higher frequency, and so on until the frequency response plot was obtained.

The input offset was measured to be 400 mV. Going through the mismatch analysis, one finds that the input offset is given by the same equation as the comparator (Equation 5-15). That is, the offset of the differential pair adds 1:1 to the op-amp offset, and the common source stage's offset is attenuated by the gain of the differential pair.

The open loop frequency response is shown below.

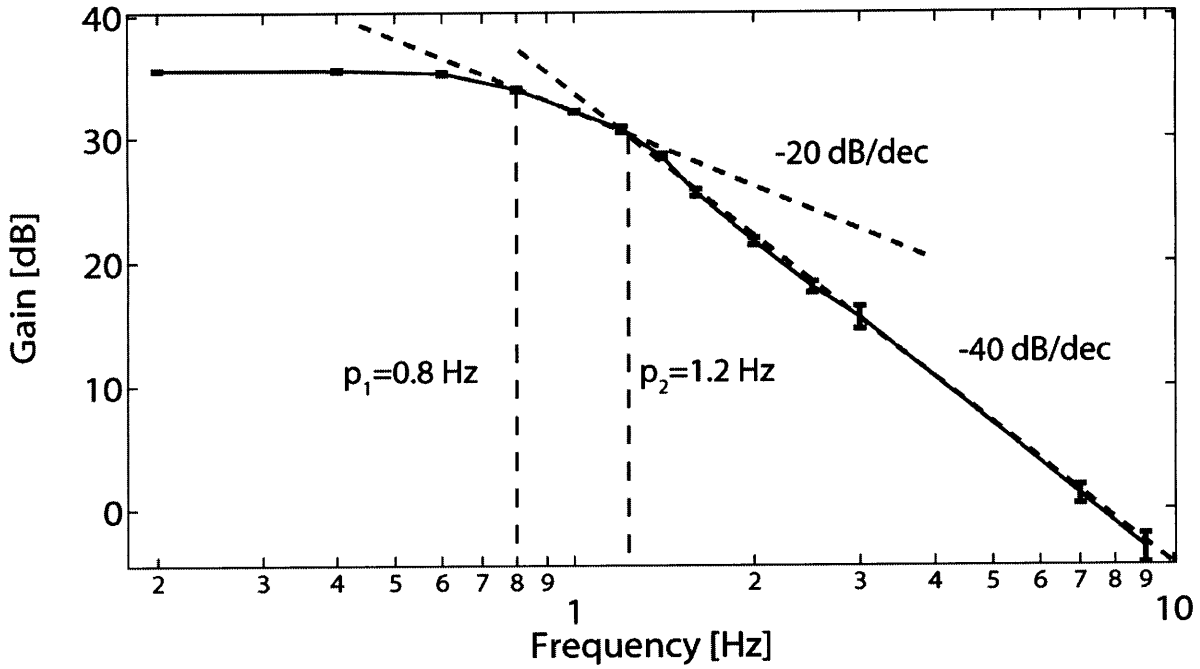


Figure 5-25: Measured open-loop frequency response for dual V_T op-amp. Dashed lines are drawn to indicate slopes of -20, and -40 dB/decade. The measured response indicated the first pole is at 0.8 Hz, and the second at 1.2 Hz. The unity gain frequency is ~ 7.5 Hz.

The measured frequency response indicates an open loop gain of 36 dB, an initial pole at 800 mHz and a second at 1.2 Hz. Hand calculations are shown later in this chapter indicating the source of these poles. This frequency response gives a unity gain frequency of 7.5 Hz, and a phase margin of ~10°.

Next, the op-amp is put in unity gain configuration, as shown.

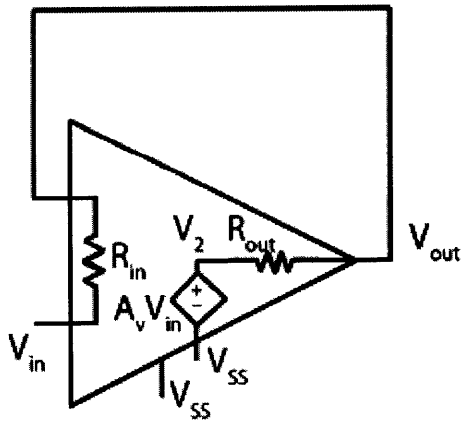


Figure 5-26: Unity gain configuration used to measure input common mode range and step response.

The step response was measured in unity gain configuration. A 500 mV step was applied by the Tektronix 3102 function generator. The measured output voltage and step are pictured.

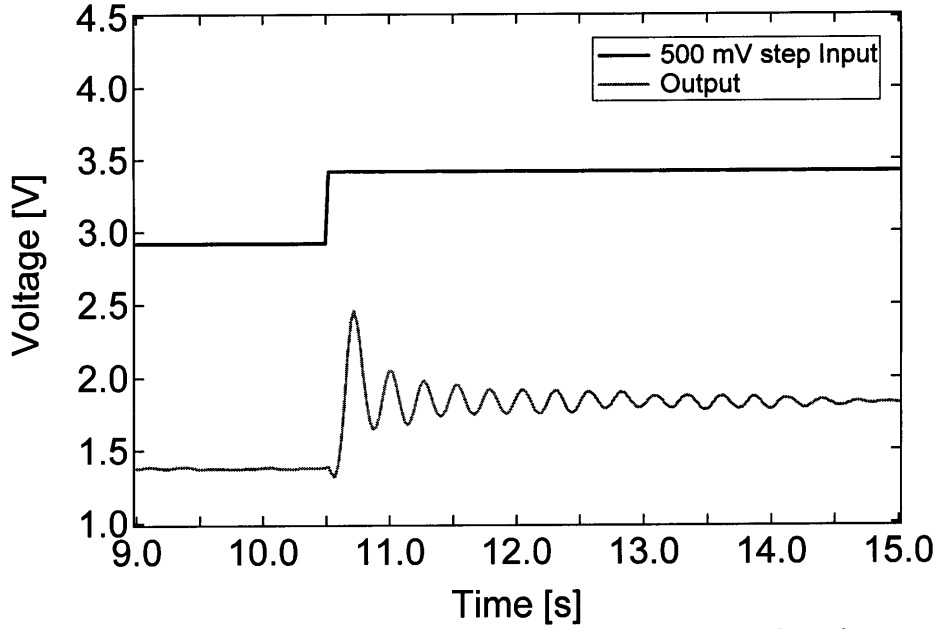


Figure 5-27: Measured step response and input step at unity gain.

The extreme overshoot indicates a very low phase margin (0-10°), as we would expect considering the frequency response in Figure 5-25. Next, the op-amp is connected in negative feedback, shown below.

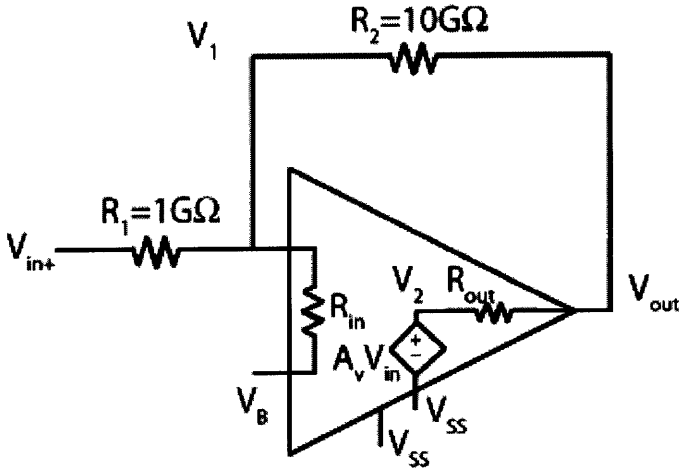


Figure 5-28: Op-amp in negative feedback with gain=-10.

The feedback resistors need to be very large due to the output resistance of the op-amp. Even though the output stage of the op-amp is a source follower, its output resistance is still ~400 MΩ. However, when the op-amp is put in feedback, the output resistance of the op-amp is divided by the gain, A_V.

Solving for the gain from V_{out} to V_{in}, one finds the following relationship.

$$\frac{V_{out}}{V_{in}} = \frac{R_2}{R_2\left(\frac{R_o + R_2}{R_o + A_v R_2}\right) + R_1\left(\frac{R_o + R_2}{R_o + A_v R_2} - 1\right)} \qquad (5\text{-}17)$$

$$\frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1} \quad when \quad \frac{R_o}{A_v} << R_2$$

For this case the effective output resistance of the amplifier is ~6 MΩ, much less than the feedback resistors.

When a step is applied to V_{in+}, an overshoot of ~20% is observed. A second order response is seen, since at a gain of 20 dB, we are past both poles. The settling time to reach 99% of the final value is approximately 1.3 seconds.

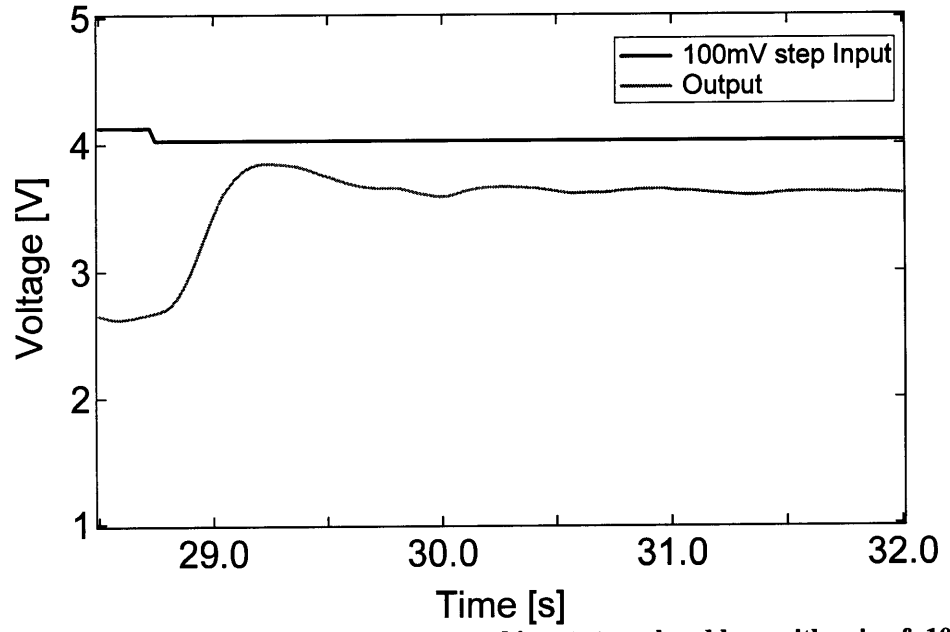


Figure 5-29: Measured step response and input step, closed loop with gain of -10.

For a second order system, the percent overshoot can be related to the quality factor (Q) of the system by the following equation [7].

$$\%\ overshoot = 100e^{\frac{-\pi}{\sqrt{4Q^2-1}}} \qquad (5\text{-}18)$$

A 20% overshoot yields a Q of 1.1 from Equation 5-18. We can then relate Q to ω_t and ω_{eq}, the unity gain frequency, and higher order pole frequency, respectively.

$$Q = \sqrt{\frac{\omega_t}{\omega_{eq}}\sqrt{1+\frac{\omega_t^2}{\omega_{eq}^2}}} \tag{5-19}$$

Using the value of 1.1 for Q, we find that $\frac{\omega_t}{\omega_{eq}}$ is equal to 0.9. Finally, this ratio can be used to calculate the phase.

$$\text{phase} = -90^o - \tan^{-1}\left(\frac{\omega_t}{\omega_{eq}}\right) \tag{5-20}$$

This yields a phase of -132° at a gain of 20 dB, close to our estimated phase of -125° from the bode plot. At 20 dB, the amplifier should be at a phase 45° higher than at unity gain, since we have a two pole system. This implies a phase margin of 3°, which agrees with our measured step response at unity gain in Figure 5-27.

The following table summarizes the performance of the op-amp.

Metric	**Value**
R_{in}	> 1 TΩ
R_{out}	400 MΩ
Input offset	400 mV
Open loop gain	36 dB
$f_{.3db}$	0.8 Hz
f_u	7.5 Hz
Slew rate [with 1 pF load]	3 V/ms
Settling time	1.3 s
Bias current	55 pA
V_{DD}	5 V

Table 5-5: Summary of typical operational amplifier characteristics

There is one operational amplifier published in literature. The following table compares the published op-amp (two topologies) with those reported here.

Author	N. Gay et al. [5]	N. Gay et al. [5]	This work
Technology	Photolithographic evaporated pentacene	Photolithographic evaporated pentacene	Photolithographic dual V_T evaporated pentacene
Topology	Nested-G_m-C-Compensation	Two-stage	Two-stage
Load	Diode-connected	Diode-connected	Zero-V_{GS}
Open Loop Gain	48 dB	40 dB	36 dB
Unity Gain Frequency	2.4 Hz	10 Hz	7.5 Hz
Unity Gain-Bandwidth Product	710 Hz	1000 Hz	473 Hz
Compensated?	yes	Unreported	no
V_{DD}	40 V	40 V	5 V
Power	Unreported	Unreported	1.7 nW

Table 5-6: Performance comparison between state-of-the-art organic operational amplifiers.

The op-amp presented in this chapter has approximately ½ the gain-bandwidth product while using an 8x lower power supply. In addition, the Infineon technology used in [5] has a 4 μm minimum channel length, which translates to an equivalent 36% load capacitance reduction compared to our 5 μm technology. In the next chapter, we will discuss a redesigned op-amp with ~2x the frequency response.

5.3.6 Op-Amp Frequency Response

We will find the dominant poles in the op-amp and compare them with measured results. We do so by first drawing the small signal equivalent circuit model of the right half of the schematic, shown in Figure 5-30.

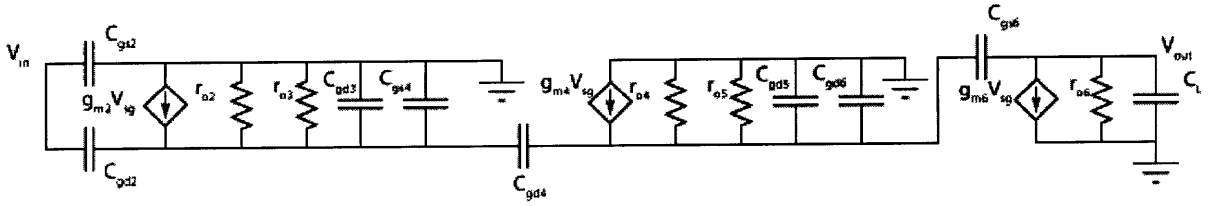


Figure 5-30: Op-amp small signal model.

We can greatly simplify the small signal model by looking at the capacitances in circuit schematic. We notice capacitances connected from input to output for all three stages. The Miller approximation will be to instead add capacitors from input to ground, and output to ground, in place of the capacitor coupling the input and output [11].

Now, we can draw a more compact small signal model.

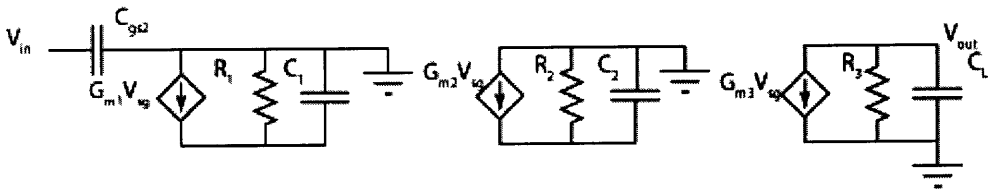


Figure 5-31: Simplified op-amp small signal model after Miller approximation.

C_1, C_2, R_1, R_2, and R_3 are given below.

$$\begin{aligned} C_1 &= C_{gd2} + C_{gd3} + C_{gs4} + (1 + A_2)C_{gd4} \\ C_2 &= C_{gd5} + C_{gd6} + C_{gd4} \\ R_1 &= r_{o2} \parallel r_{o3} \\ R_2 &= r_{o4} \parallel r_{o5} \\ R_3 &= r_{o6} \end{aligned} \tag{5-21}$$

We will use the open circuit time constant (OCTC) method to find the -3db frequency [11]. C_L and C_{gs2} are found to have very small time constants, so we will focus our attention to C_1 and C_2.

$$f_{-3db} = \frac{1}{2\pi(R_1C_1 + R_2C_2)} = \frac{1}{2\pi(240G\Omega * 940fF + 357G\Omega * 409fF)} = .430Hz \tag{5-22}$$

This number is in close agreement with that obtained from the Bode plot. The load capacitances are almost entirely due to parasitic overlap capacitances. This also implies that the poles are dependent on the run-to-run alignment between layers. Therefore, the poles can change by as much as 2x depending on the accuracy of alignment. The next chapter discusses the limitations on the frequency response, and suggests ways to improve it. We also outline the design of a faster, compensated op-amp.

5.4 Summary

Digital circuits were implemented using the dual V_T process. The design of area-minimized inverters was described. Positive noise margin inverters were demonstrated using a 3 V supply and picowatts of power. A rail-to-rail 11-stage ring oscillator was measured, indicating an inverter propagation delay of 27 ms. The supply and power consumption are record lows for integrated organic circuits.

A differential pair was fabricated and measured to have a differential voltage gain of 23.5 dB at a common mode voltage of V_{CM}=3.4 V, and a common-mode rejection ratio of 23 dB. An input offset of 200 mV was measured.

A comparator consisting of a differential amplifier and latch was tested. The comparator was measured to have an input offset 200 mV while using 5 nW and a 5 V supply.

A two-stage uncompensated operational amplifier was designed and measured to have an open loop gain of 36 dB, and a unity gain frequency of 7.5 Hz , dissipating less than 2 nW at a 5 V supply.

These proof-of-concept circuits demonstrate the feasibility of OTFTs for mixed signal circuits. The following chapter will discuss methods to improve the performance of these circuits.

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Chapter 6 Improving Organic Circuit Performance

In this chapter, techniques to improve the operational amplifier and comparator performance are discussed. A design for a faster, compensated organic op-amp is presented, as well as a comparator that can be clocked at higher frequencies.

Parasitic overlap capacitance is found to be the technological limitation to increased frequency response of organic circuits in the current technology. Methods for improving the performance include scaling the channel length, reducing overlap capacitance, increasing mobility, and increasing the ΔV_T.

A self-aligned process using a novel backside exposure technique is introduced, and shown to reduce the parasitic overlap capacitance almost an order of magnitude, compared to the standard 5 μm overlap process. In addition, we present a dielectric annealing process, created by *Ryu et al.*, that has been shown to increase mobility by 2-3 times. Not only does the dielectric anneal improve mobility, the combination of a parylene-N dielectric and annealing has been shown to increase the ΔV_T. The impact of these technological improvements on circuit performance is discussed.

6.1 Improving Operational Amplifier Performance

In a CMOS op-amp, one could increase frequency response at the cost of higher power by increasing the bias current. Below a CMOS differential pair is pictured next to the implemented organic version with zero-V_{GS} loads.

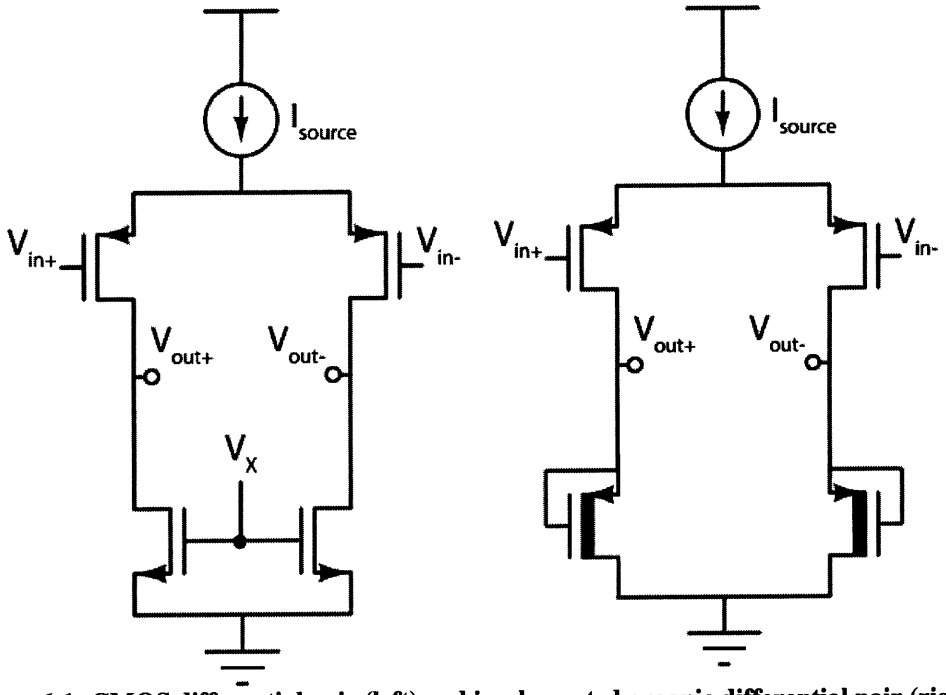

Figure 6-1: CMOS differential pair (left) and implemented organic differential pair (right).

Normally, one can extend the bandwidth of an amplifier by increasing the current. Since the amplifier's pole will be proportional to the effective resistance times the load capacitance, higher currents will lower the effective resistance and decrease the associated time constant. If we wish to increase the current in the CMOS differential pair, we can increase I_{source} and simply raise V_X, increasing the loads' overdrive so that the output voltage remains at the same common-mode level. In the organic version, if we increase the bias current, we must make the zero-V_{GS} loads appropriately wider to have the same output voltage. The zero-V_{GS} devices' C_{GD} loads the output, due to the parasitic overlap capacitance between the gate and drain. At some point, any increase in current gives no increase in frequency response, since the load capacitance is dominated by the zero-V_{GS} C_{GD}.

This behavior is illustrated in Figure 6-2, where the gain-bandwidth product (gain * -3dB frequency) of the op-amp is plotted versus bias current in the differential pair.

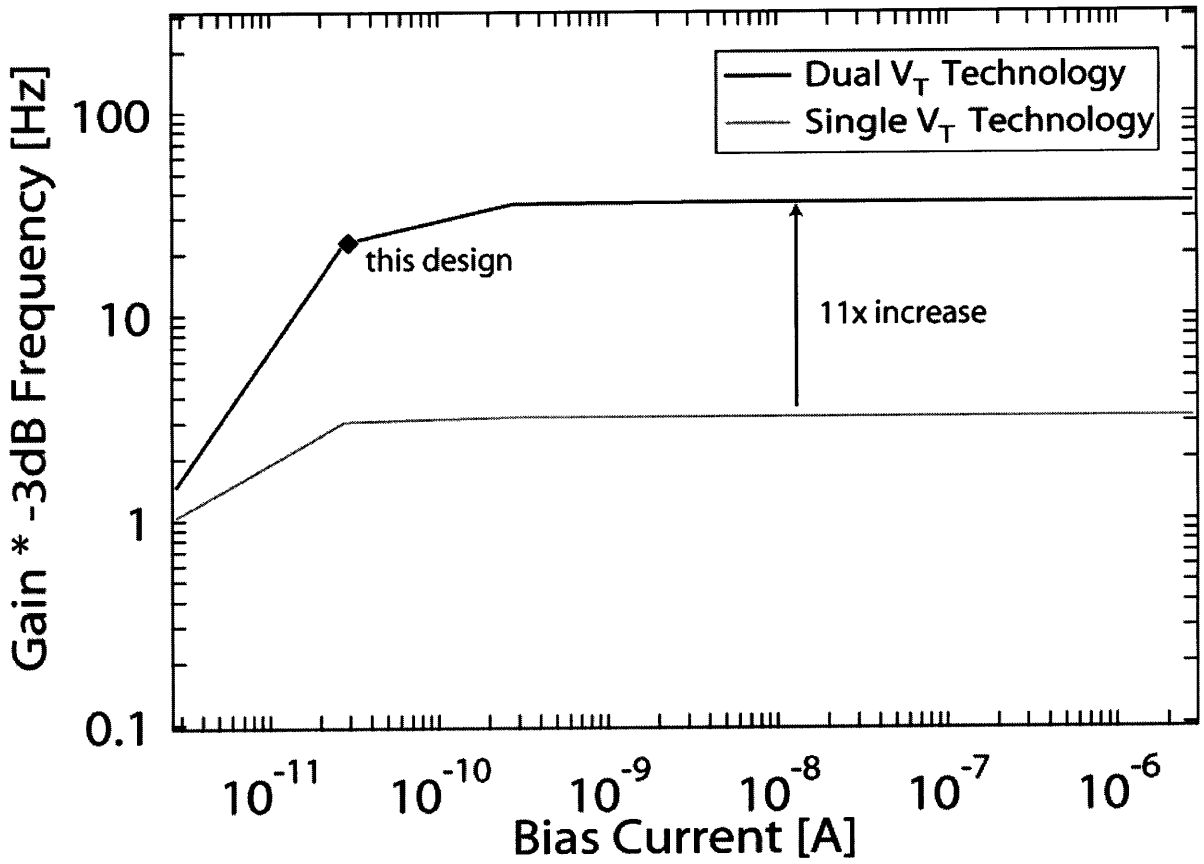

Figure 6-2: Gain*-3db frequency versus bias current. Implemented op-amp design indicated by diamond.

There are a few noteworthy points to take from this plot. First, the implemented op-amp design could have its frequency response increased by approximately 56% by increasing the bias current to 550 pA. Of course, the input pair and loads would be wider than the initial implementation in order to maintain the same gain, and common-mode output. The larger load capacitance is taken into account at each bias current. The load capacitances at the output stages are almost entirely due to parasitic overlap.

This plot also indicates that the dual V_T technology offers an impressive improvement in frequency response. The first stage pole is determined by the parasitic overlap of the input device and zero-V_{GS} load. Since the "high" V_T device sinks more than an order of magnitude more current at zero-V_{GS} than the "low" V_T device, the frequency response of the dual V_T implementation is better than a single V_T topology. The frequency response doesn't receive the full 30x improvement because the large input pair contributes significantly to the load capacitances.

More improvement from the dual V_T technology could be obtained by using a lower gain differential pair, which would require a lower g_m and therefore smaller input pair. This would make the zero-V_{GS} device contribute a higher percentage to the total load capacitance

at each stage. Also, if the high V_T device could be made with an even more positive V_T, the frequency response could be further improved.

With this in mind, we will describe the optimal design for a compensated op-amp in this technology. First, the current through both stages must be increased by 10. This requires increasing the width of the zero-V_{GS} loads by 10. In addition, the driver devices must be sized 10x larger, to provide the same gain at the higher bias current.

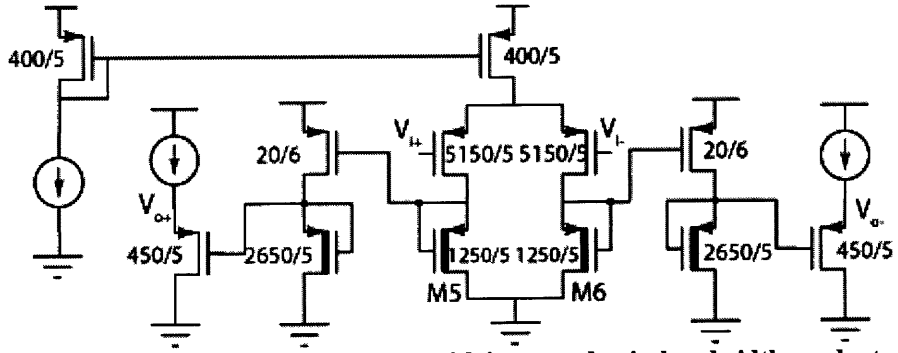

Figure 6-3: Uncompensated op-amp with improved gain-bandwidth product.

We now wish to add compensation to achieve 45° phase margin. To do so, we will put a capacitor, C_c, between the input and output of the second stage. Its capacitance will be multiplied by $1+A_{v,2}$ by the Miller effect, and will be added to the output node of the first stage, pushing this pole lower. In addition, at higher frequencies, C_c will look like a short, effectively making the input to the second stage look like a diode-connected device. This will push the second pole out, because the output resistance it sees will be $1/g_m$.

To provide a 45° phase margin, we choose our compensation capacitor with the following equation [1].

$$C_C = C_2\left(\frac{g_{m2}}{g_{m4}}\right) = 31pF \tag{6-1}$$

Since our C_{ox} is ~$2x10^{-16}$ F/μm^2, this compensation capacitor would be implemented by a MIM capacitor of dimension 393x393 μm^2.

We can now calculate the two poles. This op-amp will have a unity gain frequency of ~ 2 Hz, ensuring a 45° phase margin.

$$\begin{aligned} p_1 &\approx \frac{1}{2\pi(35G\Omega * 372pF)} = .03Hz \\ p_2 &\approx \frac{1}{2\pi(2.1G\Omega * 31pF)} = 2.4Hz \end{aligned} \tag{6-2}$$

The final schematic is shown below.

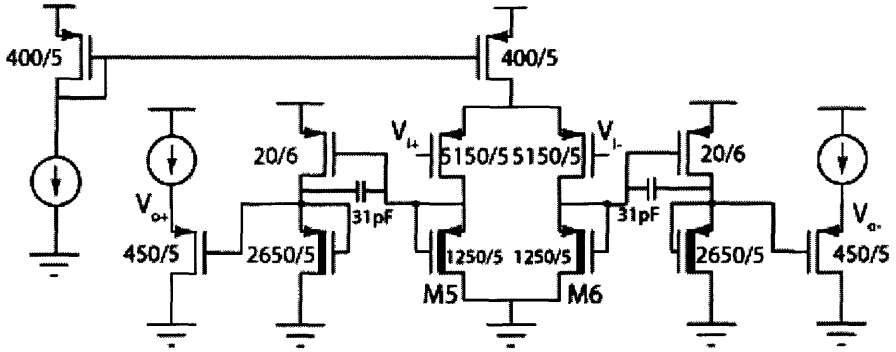

Figure 6-4: Compensated op-amp with improved gain-bandwidth product and 45° phase margin.

Further enhancement of the frequency response can be achieved by improving the OTFT technology. The proposed technology improvements are listed here:

1. Scale channel length
2. Reduce parasitic capacitance
3. Increase mobility
4. Increase ΔV_T

These four improvements will be discussed at the end of the chapter.

6.2 Improving Comparator Performance

Chapter 5 described a comparator with 200 mV offset and latching time of 32 ms. If the comparator is to be used in a flash ADC, both the clocking speed and input offset must be improved to enable medium resolution ADCs at reasonable sampling frequencies.

As described in Chapter 5, the latch time constant in the comparator is given by $\tau = \frac{C_L}{g_m}$, where g_m is the transconductance of the inverter driver, and C_L is the load capacitance at the outputs of the latch. To decrease the latch time constant, we can increase g_m by increasing the current through the inverter. This is done by increasing the width of the zero-V_{GS} load. Additionally, the W/L of the driver must be increased proportionally, in order to keep the inverter trip point at $V_{DD}/2$. Of course, C_L will also increase as the sizes of these devices are made larger. Figure 6-5 plots the trend of the latch time constant versus the current in the inverter. We note that the measured comparator operated at higher currents than the op-amp due to wafer-to-wafer variation. Therefore, we use the same current as the op-amp to enable easier comparison.

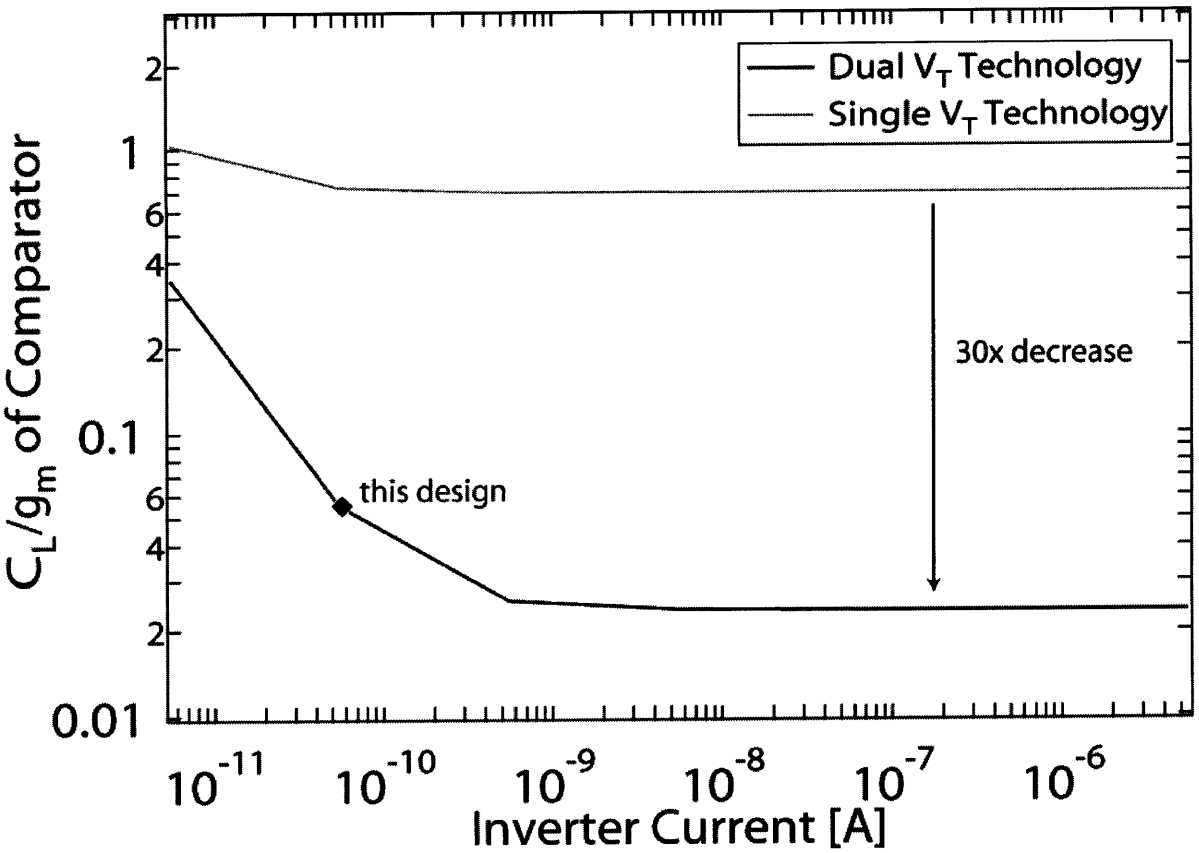

Figure 6-5: Latch time constant versus inverter current. Implemented design indicated by diamond.

As was the case with the op-amp, increasing the current through the latch eventually provides no further benefit, as the zero-V_{GS} load completely dominates the load capacitance. Since the high V_T device sinks ~30x more current than the low V_T device, the dual V_T implementation translates to a 30x decrease in the latch time constant. The full 30x benefit of the dual V_T technology is obtained here, because the zero-V_{GS} is always much wider than the driver, in order for the inverter to trip at $V_{DD}/2$.

The dual V_T latch time constant could be lowered by a factor of 2.2 by increasing the inverter current 100x. Unfortunately, increasing the current while maintaining the same gain does not reduce the offset. This is because the ratio of g_m's and overdrive are constant in Equation 5-14. The offset could be reduced by decreasing V_{DD} – this would require the driver to be sized wider to still trip at $V_{DD}/2$. Doing so would decrease the ratio of g_m's and overdrive in Equation 5-14.

Shown below is an improved comparator design. The inverters in the latch now use 100x more current, achieving a C_L/g_m of 0.025 s. The input stage also has been resized, as its time constant must be decreased to enable the comparator to be clocked faster. The amplifier provides the same gain as the initial implementation. Only one inverter is used to delay the clock signal. Therefore, the amplifier and latch are only on together for one inverter delay. These nodes are fully charged when the latch turns on, therefore there is no extra time required for the latch to receive the correct voltages from the amplifier. In fact, the time both

stages are on should be minimized, because during this time the outputs are being driven by both the amplifier and latch. Because of this, the latch should be designed so that it overpowers the differential pair during this period, and starts driving the outputs to the voltage rails. Therefore, in this implementation, the $g_{m,latch} > g_{m,differential\ pair}$.

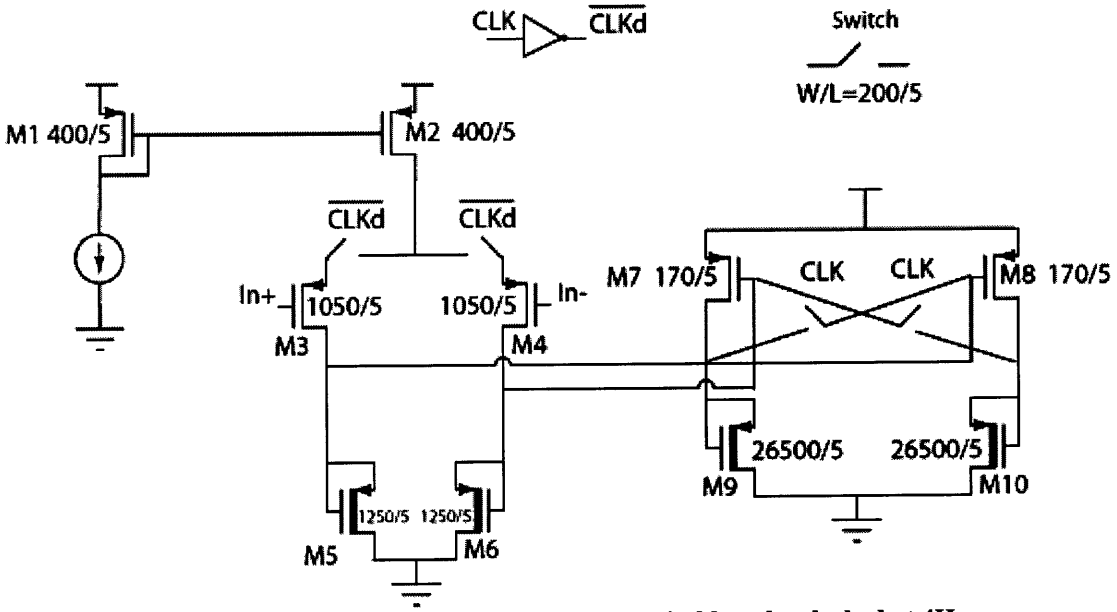

Figure 6-6: Improved comparator, suitable to be clocked at 4Hz.

$$t_{amplifier} \leq inverter\ \ delay + t_{latch}$$
$$t_{amplifier} \leq 27ms + 82ms \qquad (6\text{-}3)$$

These results indicate that the comparator could be clocked at 4 Hz assuming the differential amplifier meets the criterion of Equation 6-3.

6.3 Self-aligned Process for Reduced Overlap Capacitance

As seen in the previous section, the parasitic capacitance from the gate to source/drain overlap dominates the load capacitance for the operational amplifier and comparator. For the inverter design described in Chapter 5, parasitics account for >50% of the load capacitance. Not only would a self-aligned process drastically improve the speed of these circuits, it would improve the reproducibility of circuit performance. As of now, the poles in the uncompensated operational amplifier and the inverter propagation delay, are determined by overlap capacitances. Likewise, the latch time constant is also determined by the overlap capacitances. Run-to-run variation in alignment can cause these overlap capacitances to change from at most 2.0-0.2x the nominal, leading to a wide variation in frequency response of these circuits.

Unlike CMOS, conventional OTFT processes are not self-aligned, due to fundamental differences in the device structure and processing. In a normal CMOS process, the gate is processed on top of the channel, and an ion implantation step is performed to define the source/drain regions. The gate serves to mask the implantation from driving into the channel, resulting in a self-aligned process. In OTFTs, the gate is typically processed below the source/drain layer, because the bottom layer of the pentacene film has improved morphology, and becomes rougher as the film grows. Also, there are no ion implantation steps during OTFT fabrication, so there is no obvious way to translate the CMOS process flow to a self-aligned OTFT process.

We have developed a process to fabricate self-aligned OTFTs using a novel backside exposure technique [2]. In this process, we are able to retain the preferred bottom gate structure while using the chromium-gold gate as a high optical density mask to define the source/drain region. The process flow is shown below.

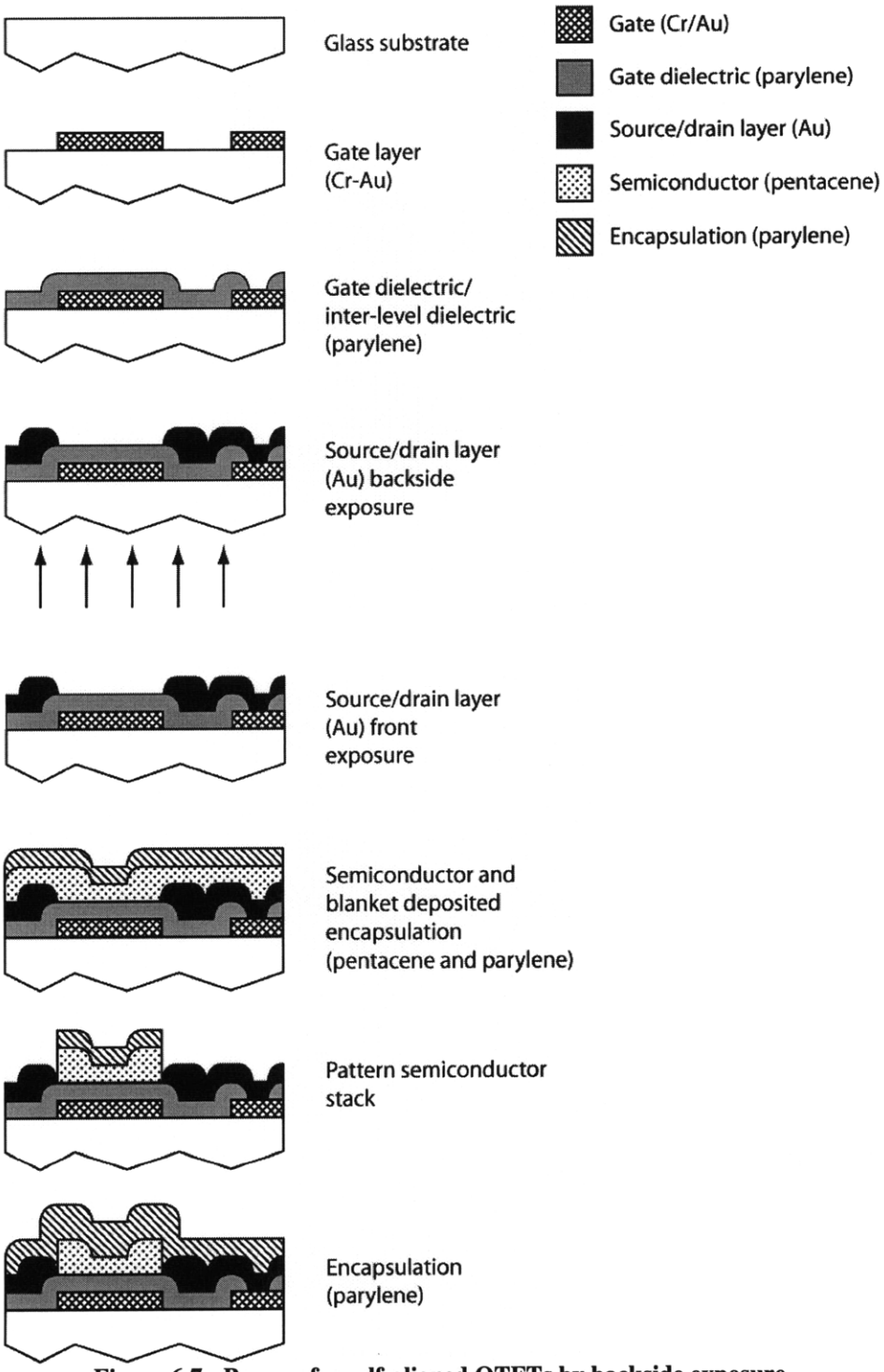

Figure 6-7: Process for self-aligned OTFTs by backside exposure.

4" borosilicate glass wafers were piranha cleaned for 10 minutes. A blanket 50 nm layer of chromium, and 50 nm of gold were electron-beam evaporated. A thicker layer of chromium is used compared to the conventional process, in order to achieve higher optical density. The

metal stack is patterned with positive photolithography and a wet etch in Transene TFA gold etchant and CR-7 chromium etchant. After a solvent strip in microstrip, a 150 nm layer of parylene-C is CVD deposited, and patterned with positive photolithography and RIE in oxygen. After another solvent strip, 40 nm of gold is e-beam evaporated. This gold layer must be both thin enough to be somewhat transparent, and also thick enough to be continuous film and conductive.

The figure below explains in more detail the backside exposure necessary for the self-aligned process.

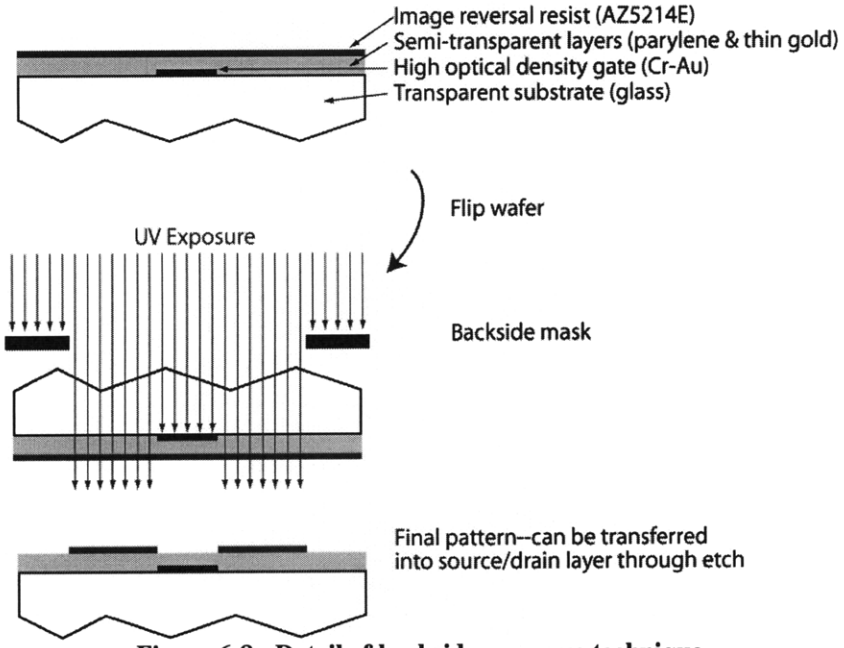

Figure 6-8: Detail of backside exposure technique.

Image reversal resist AZ5214E is spin cast at an RPM of 500 RPM for 5 seconds, 750 RPM for 5 seconds, and 3000 RPM for 30 seconds. After a prebake of 20 minutes at 95°C, the wafers were loaded into the aligner bottom-side up (i.e. gate facing up). The wafer was exposed for 250 seconds, approximately 150 times longer than a typical exposure. The long exposure was performed accounting for the relatively small percentage of light that was transmitted through the 40 nm thick gold layer to the photoresist. In the optical path of the gate, the photoresist was unexposed, thereby defining the source-gate and drain-gate edge in the resist. The wafer was then flipped, and exposed for 1.6 seconds with an additional source/drain mask, used to pattern the interconnects in the source/drain level. After a postbake at 120°C on a hotplate for 90 seconds, the wafer was flood exposed for 60 seconds, and developed. Wafers were then etched in Transene TFA, finishing the source/drain pattern. The rest of the process is identical to the standard OTFT process described in Chapters 1 & 2.

A micrograph of two finished self-aligned devices is pictured in Figure 6-9.

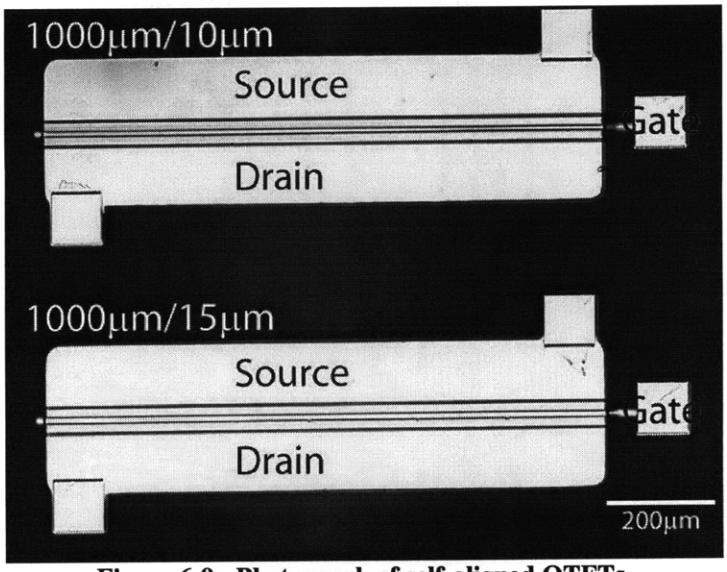

Figure 6-9: Photograph of self-aligned OTFTs.

Devices were electrically characterized with an Agilent 4156C, and the C-Vs of widths of 1000 μm and variable channel lengths are shown below. $C_{overlap}$ in Figure 6-10, is the sum of the parasitic capacitances on the source and drain side. The overlap capacitance is measured to be 0.15 fF/μm of channel width. Compared with the standard process' (overlap of 5 μm) capacitance of 1.1 fF/μm, this represents a reduction of almost 90%.

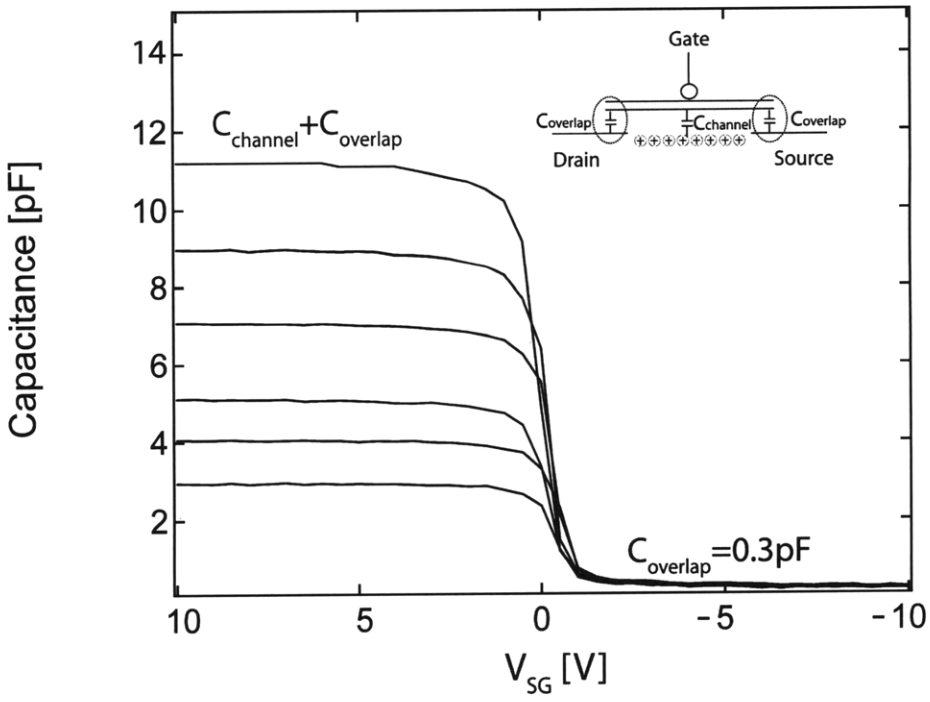

Figure 6-10: C-Vs of width=1000 μm, length=5-25 μm.

Although a large decrease in overlap capacitance is observed, the contact resistance is found to be much higher than the typical process. Any over-etch during the gold process will result in a stagger between the gate and source/drain. These un-gated regions of pentacene are extremely resistive, and appear as large contact resistances. Figure 6-11, shows a dark field image of an OTFT, indicating the gap between the gate and source/drain.

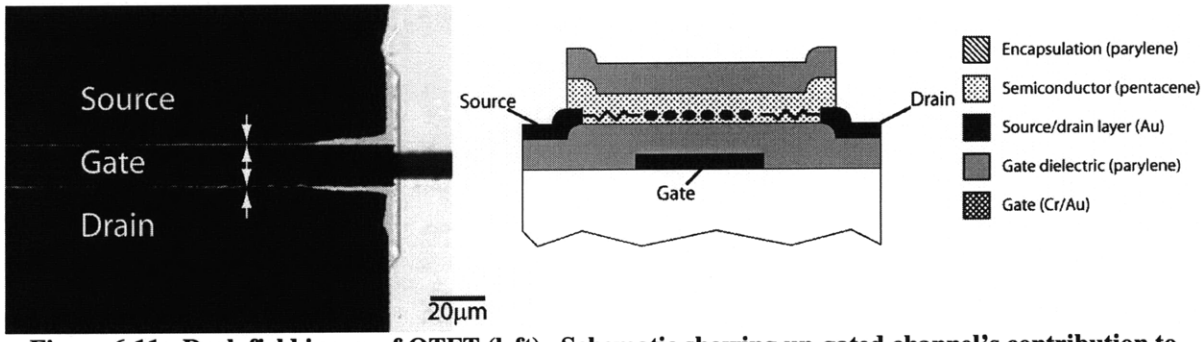

Figure 6-11: Dark field image of OTFT (left). Schematic showing un-gated channel's contribution to contact resistance (right).

Contact resistance is typically measured using the transmission line method (TLM), which requires the contact resistance to not dominate the total resistance of the FET during linear operation. Due to the extremely high contact resistance, which can be seen by the non-linear behavior at low V_{SD} in Figure 6-12, the contact resistance could not be extracted.

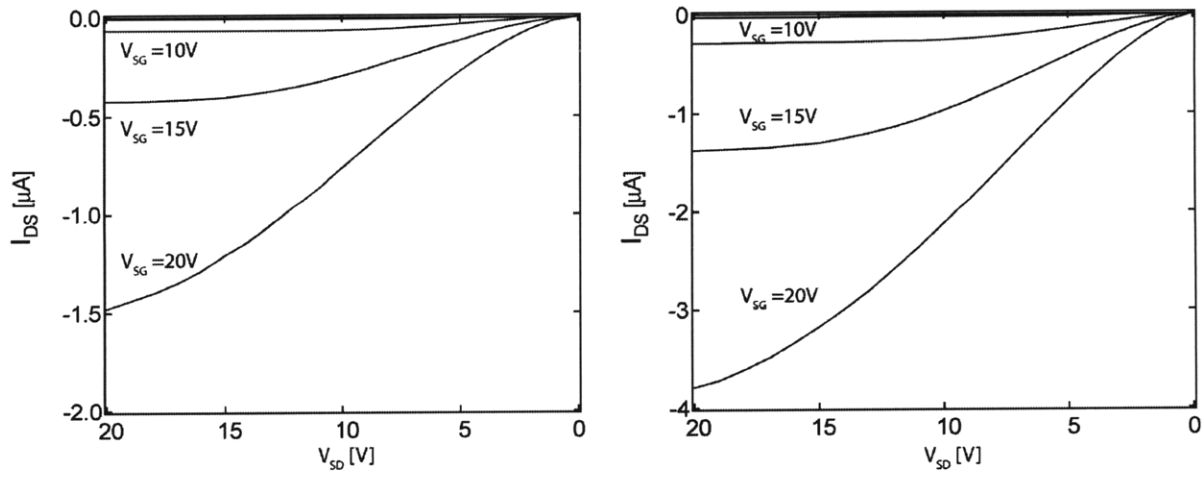

Figure 6-12: I-Vs for W=1000 μm, L=15 μm devices, 250 s exposure (left), 400 s exposure (right).

The contact resistance can be improved by increasing the backside exposure duration, with the drawback of increasing $C_{overlap}$. As seen in Figure 6-12, a 400 s backside exposure results

in improved linear characteristics, and larger saturation current. The parasitic overlap capacitance increases from 0.15 fF/ μm to 0.5 fF/ μm.

Although further experiments are necessary to optimize the process, these results demonstrate the feasibility of a self-aligned OTFT process with significantly reduced parasitic capacitances. Further work is necessary to reduce the contact resistance while minimizing the overlap capacitance.

6.4 Parylene Annealing for Improved Mobility and ΔV_T

Increasing the mobility in the OTFT will also improve frequency response. For the same W/L device (and therefore gate capacitance), a higher mobility will drive higher currents, allowing the OTFT to operate at higher frequencies.

The effect of the dielectric material on the morphology and mobility of pentacene has been widely studied [3-5]. The mobility in organic TFTs is strongly correlated with both the surface energy and roughness of the dielectric layer. Reduction in the root mean squared (RMS) roughness and lowering of the surface energy has been reported to increase the field-effect mobility in the pentacene channel, as these techniques lead to the growth of higher quality pentacene thin films. *Ryu et al.* have demonstrated that annealing prior to pentacene deposition lowers the parylene-N surface energy [6]. No change in surface roughness is measured. The completed devices exhibit mobilities approximately two times higher than those that were not annealed. In addition, annealed devices have improved resistance to bias stress degradation. The improvement in electronic performance is believed to be due to the evaporation of water, resulting in improved pentacene morphology.

A dual V_T process was completed using a parylene-N anneal prior to depositing the semiconductor. Wafers were annealed at 120°C in a nitrogen backfilled oven. The process is pictured below.

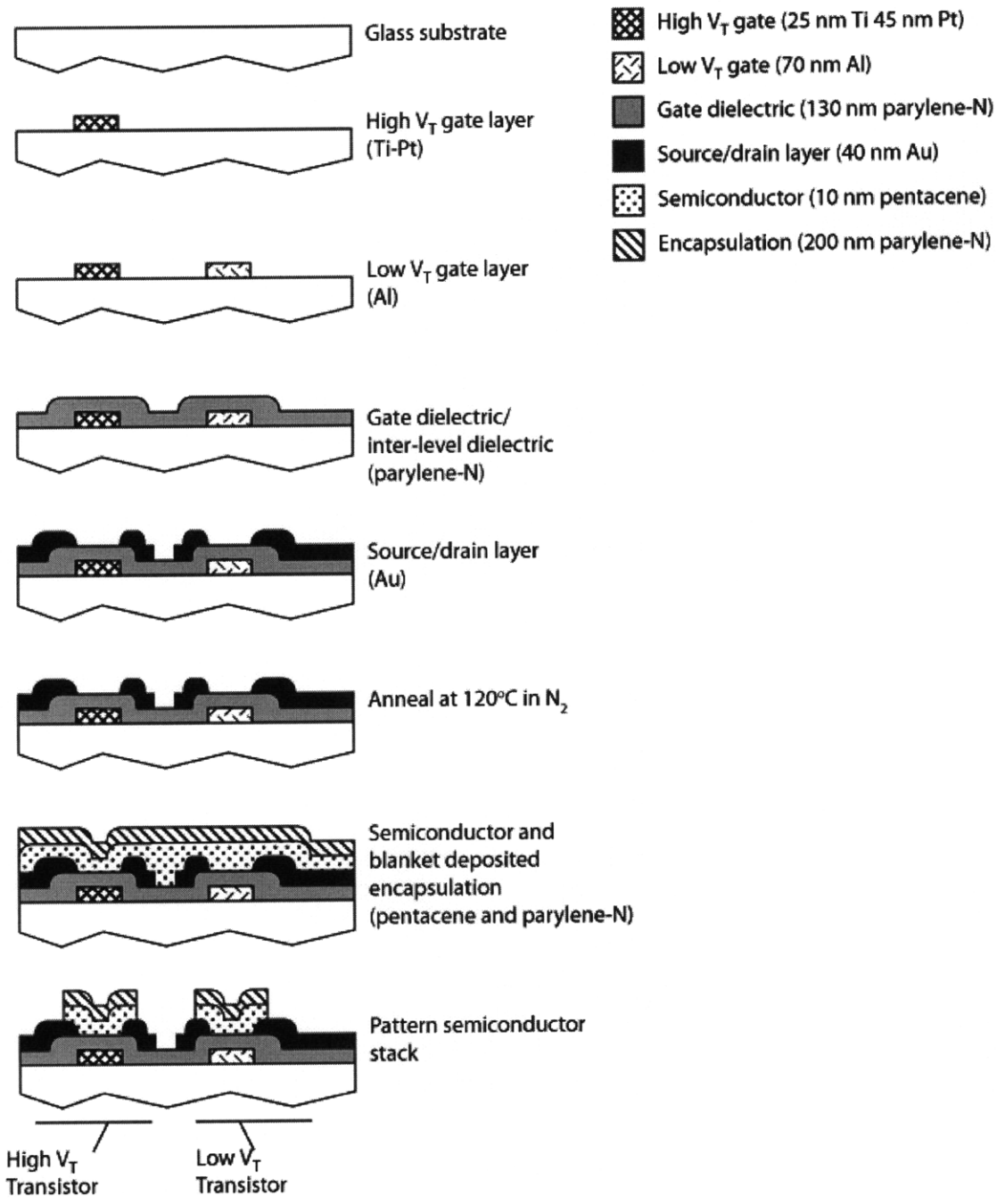

Figure 6-13: Process flow for dual V_T OTFTs with enhanced mobility.

Anneals of 10 and 45 minutes were tested. The characteristics of these wafers are summarized in the table below.

Parameter	Wafer 1	Wafer 2
Anneal time	10 min.	45 min.
Al Gate Mean V_T	-1.26 V	-0.96 V
Al Gate Std. Dev. V_T	0.15	0.11
Pt Gate Mean V_T	+0.26 V	+0.6 V
Pt Gate Std. Dev. V_T	0.15	0.12
Mean ΔV_T	1.52 V	1.56 V
Std. Dev. ΔV_T	0.04	0.05
Mobility [cm^2/Vs]	0.046	0.061

Table 6-1: Characteristics of dual V_T wafers annealed prior to pentacene deposition.

These results indicate an improvement in mobility of ~2x , consistent with results from single V_T wafers fabricated using the same dielectric anneal.

In addition, the observed ΔV_T in these wafers was substantially higher than the dual V_T process with parylene-C described in Chapter 4. The larger ΔV_T may be due to fewer interface states between the metal surfaces and the dielectric, thereby decreasing the effect of any Fermi-level pinning. More experiments are necessary to explain the origin of the larger ΔV_T.

6.5 Effect of Process Improvements

Earlier in the chapter, it was found that the operating frequencies of the operational amplifier and comparator are limited by the OTFT technology. There are four ways to improve the technology to enable higher performance OTFT circuits. These are,

1. Scale channel length
2. Reduce parasitic capacitance
3. Increase mobility
4. Increase ΔV_T

Scaling the channel length while maintaining the same W/L allows one to keep the same current drive while reducing the total area. Therefore, the circuit delay decreases with the channel length by at most A^2, where $A = L_{initial}/L_{final}$ .The 5 μm channel length in this technology can be scaled to an estimated 1 μm, where it is then limited by the lithography tools available. 1 μm channel lengths have been fabricated for lateral photoconductors, but 1 μm OTFTs have not yet been processed [7]. Reducing the channel length from 5 to 1 micron would increase circuit operating frequency by 25.

Overlap capacitance contributes the majority of the load capacitance for the circuits described. If we assume the overlap capacitance is 100% of the load capacitance, a reduction in overlap capacitance of A will increase speed by A.

By increasing the carrier mobility, one can achieve the same current drive at a lower W/L. For instance, a device with 2x mobility and a W/L of 5 would source the same current as a device with a W/L of 10 and mobility of 1. Therefore, an increase in mobility of A reduces the circuit delay by A.

Lastly, increasing the ΔV_T between the low and high V_T devices will increase circuit speed. Since the high V_T zero-V_{GS} load must be sized much wider than the low V_T driver, increasing the V_T difference between the devices reduces the relative strength of the low V_T device to the high V_T device. This allows the width of the zero-V_{GS} load to be sized smaller, thereby decreasing the load capacitance. The speed increase with respect to an increase in ΔV_T depends on the values of both devices' threshold voltages.

Processing methods for reducing the parasitic capacitance, improving mobility, and increasing ΔV_T were demonstrated. Here, we will see the effects of these process improvements on the op-amp and comparator performance.

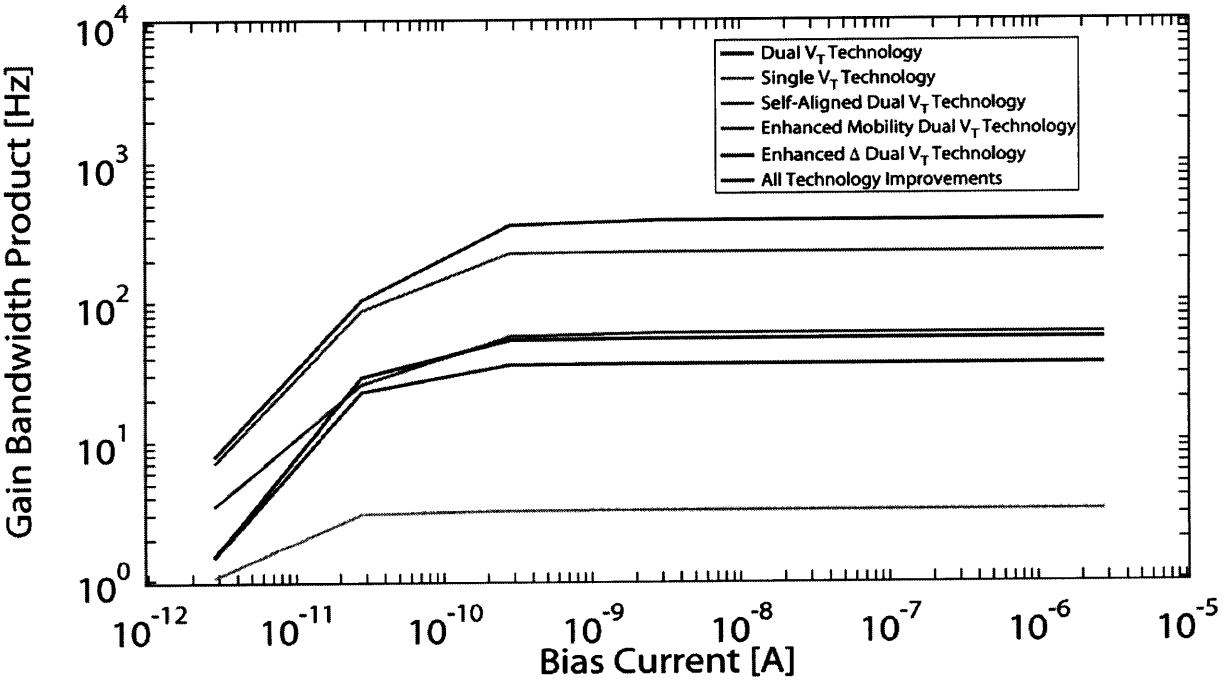

Figure 6-14: Process improvements on maximum gain *-3dB frequency.

Figure 6-14 plots the gain-bandwidth product versus bias current. To get the full benefit of these process improvements, the amplifier bias currents must be significantly higher than the nominal case. This is because the process improvements have reduced the effect of the C_{GD} of the zero-V_{GS} device on the total load capacitance. Therefore, the zero-V_{GS} limits the performance at higher currents than previously.

If all the process improvements are implemented, the maximum estimated gain-bandwidth product increases ~150x. These technology improvements could increase the compensated op-amp's unity gain frequency from 2 Hz to over 300 Hz.

The same analysis applies to the case of the comparator. Here, the technology improvements reduce C_L/g_m by 450x from the nominal case. The improved technology could enable comparators clocked as high 1.8 kHz.

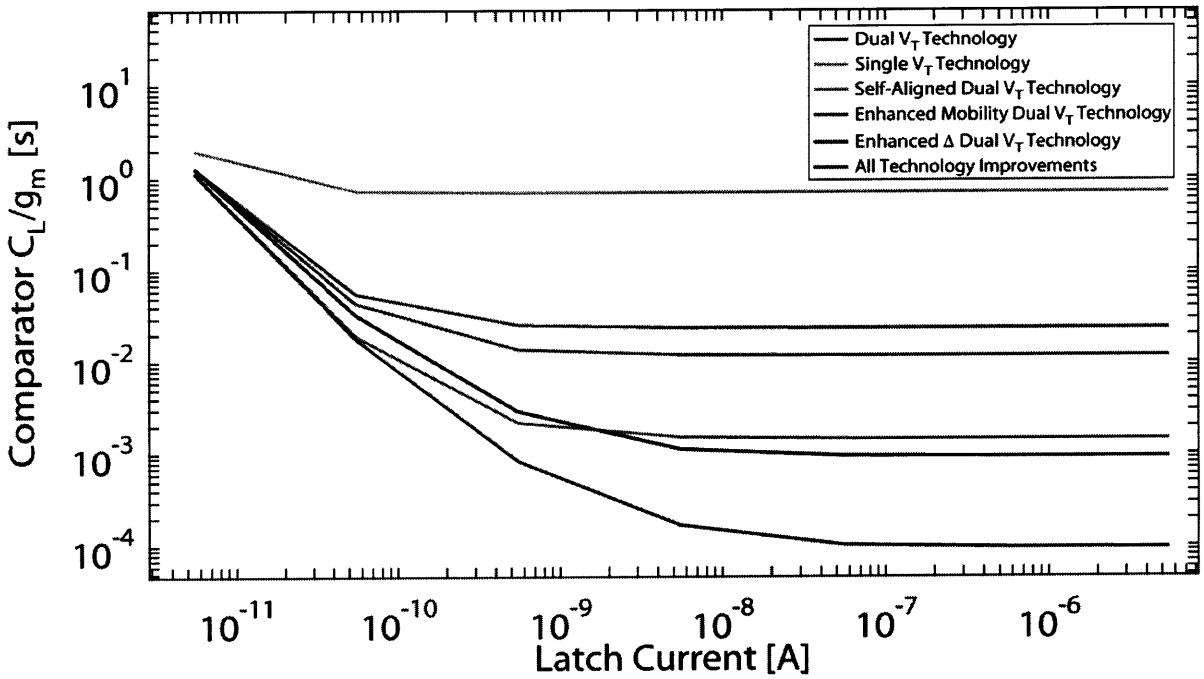

Figure 6-15: Process improvements on C_L/g_m of comparator.

6.6 Summary

This chapter described the trade-offs between bias current and frequency response in the dual V_T technology. The zero-V_{GS} load's parasitic capacitance was found to limit the speed of both the op-amp and comparator. An improved, compensated op-amp design was presented, as was a faster comparator.

The speed of OTFT circuits could be increased by a number of technological improvements. These include: decreasing the channel length, increasing mobility, lowering parasitic capacitance, increasing the ΔV_T.

A process for self-aligned OTFTs was presented. Wafers fabricated using the process were found to have parasitic capacitances almost an order of magnitude lower than the standard 5 μm overlap technology.

In addition, dual V_T wafers were demonstrated with 2x higher mobility, and a 1.5 V ΔV_T. These results were obtained using a parylene-N gate dielectric, and a pre-pentacene deposition anneal in nitrogen.

In total, these technological improvements could increase the maximum frequency response of the op-amp and comparator by 150x and 450x, respectively.

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Chapter 7 Conclusion and Future Work

This thesis has proven the feasibility of organic thin-film transistors in active-matrix systems and mixed signal integrated circuits. An organic-active matrix imager, suitable for large-area and flexible optoelectronics was demonstrated with an inkjet printed photoconductor. In order to design more complicated OTFT circuits, a model and simulation framework was implemented in MATLAB. The inverter circuit was chosen as a fundamental building block with which to investigate trade-offs in OTFT circuit design. It was shown through simulation that zero-V_{GS} loaded inverters offer significantly better performance than the diode-loaded topologies. Simulations also revealed the area and lifetime benefits of lowering the power supply. A dual threshold voltage process was motivated by its area and speed improvements for OTFT circuits.

A low temperature, integrated dual threshold voltage process was designed, suitable for fabricating large-area flexible ICs. Using a high work function metal (Pt) and low work function metal (Al) gates, devices were found to be nominally identical, but shifted by an amount ΔV_T. A ΔV_T of 0.6 V was reproduced on multiple wafers. It was found that a substantial and reproducible ΔV_T was attainable only by using lift-off to pattern the metal gates.

Area-minimized digital circuits were designed and tested. An inverter with positive noise margins and a rail-to-rail ring oscillator were demonstrated using a 3 V supply, the lowest reported for large-area integrated OTFT circuits. The power consumption of these digital circuits were orders of magnitude less than the state-of-the-art in literature. A differential amplifier, operational amplifier, and comparator were fabricated and tested. The differential pair was found to have a differential gain of ~23 dB, and a CMRR of 23 dB. The dual V_T differential amplifier is this highest gain amplifier reported, and uses an order of magnitude lower V_{DD} than any other.

The uncompensated operational amplifier was measured to have an open loop gain of ~ 36 dB, input offset of 400 mV and a unity gain frequency of 7.5 Hz. The comparator was measured to have an input offset ~200 mV.

Improved designs for the operational amplifier and comparator were discussed. Both circuits could have their frequency response improved with the current technology, at the expense of

increased power consumption and larger area. The overlap capacitances were found to limit the maximum frequency response of the circuits. Four ways to improve the technology were presented: scaling the channel length, increasing the mobility, reducing the overlap capacitance, and increasing the ΔV_T. A novel backside exposure technique for self-aligned OTFTs was introduced, and shown to reduce overlap capacitance by an order of magnitude. In addition, a parylene-N dielectric and pre-pentacene anneal were observed to increase the mobility by 2-3x, and the ΔV_T to 1.5 V. These three technological enhancements could increase the switching speeds of the op-amp and comparator by 150x and 450x, respectively.

7.1 ***Technological & Circuit Directions***

This section will outline proposed further technological & circuit improvements for OTFT ICs.

- Increase mobility. Even with a dielectric anneal, the mobility of our OTFTs is at best ~0.06 cm^2/Vs. Pentacene OTFTs in literature have reported mobilities as high as 3 cm^2/Vs [1]. An order of magnitude increase in the field-effect mobility, to 0.6 cm^2/Vs , should be attainable. Improving the morphology of the pentacene layer, and the interface between the dielectric and pentacene are keys to higher mobilities. Optimizing dielectric deposition to reduce roughness should be investigated. The RMS roughness of parylene should be reduced to ~1 nm or lower [2]. Surface treatments of the polymer dielectric may also prove beneficial.
- Decrease the channel length to 1 μm. Scaling the channel length by a factor of five would decrease area and load capacitance by as much as 25. In order to keep the same electrostatics, the gate dielectric thickness would need to be thinned to 24 nm. Parylene layers this thin can be obtained, but it is unclear what gate leakage currents to expect. Another approach would be to deposit a high-κ dielectric such as HfO_2 and deposit a thin layer of parylene on the surface, to have the same dielectric-semiconductor but higher gate capacitance. Techniques similar to this have been reported in literature [3].
- Shift high V_T devices more positive. By making the high V_T device more depletion-like, it can source more current at zero-V_{GS}. This reduces circuit area and parasitic capacitances. In addition, and perhaps most importantly, it will lower the input referred offset, since the zero-V_{GS} loads will now be biased in above-threshold. Therefore, any variation in V_T will have a smaller effect on current than if the device were bias in subthreshold. If these devices are to be used for the resistor string in a flash ADC, this would result in a smaller variation of resistor values.
- Employ offset cancellation in the comparator. The resolution of an organic ADC is severely limited if one can at best achieve a comparator with 200 mV offset with a 5 V supply. The latch offset can be attenuated by increasing the amplifier gain, but any offset in the differential pair will still remain. Therefore, input offset storage (IOS) or output offset storage (OOS) techniques must be used to measure and subtract the offset from the comparator if one wishes to resolve 4 bits or greater [4].

REFERENCES FOR CHAPTER 7

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Appendix A: OTFT Model

The following model is an adapted amorphous silicon model used to simulate the current-voltage characteristics of the OTFT.

$$I_D = \frac{W}{L} q\mu V_{SDE} N_{HOMO} \exp\left(-\frac{E_{F0} - E_{HOMO}}{kT}\right) t_m \frac{2kT}{2qV_{trap} - kT} \left(\frac{t_m \varepsilon_{ox} V_{GTE}}{t_{ox} \varepsilon_s V_{trap}}\right)^{\frac{2qV_{trap}}{kT}-1} \quad \text{(A-1)}$$

$$V_{SDE} = \frac{V_{SD}}{\left(1+\left(\frac{V_{SD}}{\alpha_{sat} V_{GTE}}\right)^m\right)^{\frac{1}{m}}}$$

$$V_{GT} = V_{SG} + V_T$$

$$V_{GTE} = \frac{V_{MIN}}{2}\left(1+\frac{V_{GT}}{V_{MIN}}+\sqrt{\delta^2+\left(\frac{V_{GT}}{V_{MIN}}-1\right)^2}\right) \quad \text{(A-2)}$$

$$\mu = \mu_0 \left(\frac{V_{GTE}}{V_\mu}\right)^n$$

$$t_m = \left(\frac{\varepsilon_s}{2qg_0}\right)^{\frac{1}{2}}$$

The table below summarizes the parameters used in the model, and their values used in the simulations.

Parameter	Units	Description	Value
α_{sat}	none	Saturation parameter	0.64
δ	none	Transition parameter from subthreshold to above-threshold	120
E_{F0}-E_{HOMO}	eV	Fermi level distance from HOMO	0.2
ε_{ox}	none	Dielectric constant of gate dielectric	3
ε_s	none	Dielectric constant of channel material	3

g_0	$cm^{-3}eV^{-1}$	Density of states at E_{F0}	10^{19}
m	None	Transition parameter to saturation	4.4
μ_0	$cm^2V^{-1}s^{-1}$	Base mobility	0.025
n	none	Mobility's exponent	1.5
N_{HOMO}	cm^{-3}	Effective density of states at HOMO	$3*10^{19}$
t_{ox}	nm	Thickness of gate dielectric	130
V_{MIN}	V	Convergence parameter for subthreshold regime	0.01
V_μ	V	Mobility V_{GTE} dependence parameter	2
V_T	V	Threshold voltage	-1
V_{trap}	V	Characteristic voltage for trap state	0.02

Table A-1: List of OTFT model parameters used in simulation.

Appendix B: Noise Margin Calculation Code

```
%%%%%%USER INPUTS%%%%%%%%%%%%%%%%
WDriverInit = 2000; %Width of Driver for first curve (set to 20 for ratio = 1)
NumCurves = 8; %number of curves you want plotted
%RatioInc = 10; %Driver Width Multiplied by this constant to make next curve (first ratio is
1 if WDriverInit =20)
NumPoints = 1000; %number of points per curve
AveWindow = 10; %number of points taken to make slope running average

VTlstart=0; %Vt of load start value
VTdstart=0; %Vt of driver start value
VtInc = -1; %both Vt's increment for each new curve
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
for count2 =1:3
VTl = zeros(0,NumCurves);
VTd = zeros(0,NumCurves);

vdd = 10;
WDriver=WDriverInit;
W=20; %for load
L=20; %for both driver and load

T=300;
k=1.38E-23;
n=1.5;
t_ox=200*10^-7;
V_mu=2;
V_TRAP=0.02;
V_SD=1;
V_SG=vdd;
q=1.6E-19;
m=4.4;
N=1.5;
AA=1.65E-8;
DD=0.62*.75;
ASAT=0.64;
DEF=0.2;
DELTA=120;
MSAT=4.4;
VO=0.021;
```

```
VMIN=0.01;

VGS=linspace(0,-vdd, NumPoints);
VDS=linspace(0,-vdd, NumPoints);
IDS=zeros(NumPoints,10);
lambda1=.02;
lambda2=.02;


NMH = zeros(0, NumCurves);
NML = zeros(0, NumCurves);
voh= zeros(0, NumCurves);
vol= zeros(0, NumCurves);
vih= zeros(0, NumCurves);
vil= zeros(0, NumCurves);
slope = zeros(NumPoints-1, NumCurves);
AveSlope = zeros(NumPoints-2, NumCurves);
figure
for count = 1:NumCurves;
for j=1:length(VGS);

VTl(count) = VTlstart + VtInc * (count -1);
VTd(count) = VTdstart + VtInc * (count -1);

VGT(j)=-VGS(j)+VTd(count);
VGTE(j)=VMIN./2.*(1+VGT(j)./VMIN+sqrt(DELTA*DELTA+(VGT(j)./VMIN-1).^2));
VSDE=-VDS./(1+(-VDS./(ASAT*VGTE(j))).^m).^(1/m);
ID=AA*WDriver/L.*VGTE(j).^N.*VSDE.*exp(-DEF*q/(k*T)).*2*k*T./(2*q*VO-
k*T).*(DD.*VGTE(j)).^((2*VO*q./(k*T))-1).*(1-lambda1*VDS);
VG=VGS;

IDS(:,j)=ID;

end
VOUT=vdd+VDS;

hold on

VGS=VDS;
VGT=-VGS+VTl(count);
VGTE=VMIN./2.*(1+VGT./VMIN+sqrt(DELTA*DELTA+(VGT./VMIN-1).^2));
VSDE=-VDS./(1+(-VDS./(ASAT*VGTE)).^m).^(1/m);
ID2=AA*W/L.*VGTE.^N.*VSDE.*exp(-DEF*q/(k*T)).*2*k*T./(2*q*VO-
k*T).*(DD.*VGTE).^((2*VO*q./(k*T))-1).*(1-lambda2*VDS);
```

```
VOUT2=-VDS;
VOUTT=zeros(1,NumPoints);
VGS=linspace(0,-vdd,NumPoints);

for j=1:length(VGS)
  dif=abs(IDS(end:-1:1,j)'-ID2);
  [x,y]=min(dif);
VOUTT(j)=y;

end
plot(vdd+VGS,-VDS(1,VOUTT))

slope(:,count)=diff(-VDS(1,VOUTT),1)/(VGS(2)-VGS(1));


%%%%%Take the running average of the slope – Low pass filter

for j=1:length(slope(:,count)) -1
   if(j>(length(slope(:,count)) - AveWindow/2))
      AveSlope(j, count) = mean(slope((j-AveWindow/2):length(slope(:,count)), count));
   elseif(j< AveWindow/2 +1)
      AveSlope(j, count) = mean(slope(1:(j+AveWindow/2), count));
   else
      AveSlope(j, count) = mean(slope((j-AveWindow/2):(j+AveWindow/2), count));
   end
end

%CALCULATE VOH, VOL, VIH, VOL
%CALCULATE NOISE MARGINS
[x2,y2]=max(abs((AveSlope(:, count))));
up=y2;
if(x2<1)
   voh(count) = 0;
   vih(count) =0;
   vil(count) = 0;
   vol(count) =0;
   NMH(count) = 0;
   NML(count) =0;
else
   while(AveSlope(up, count)<-1 && up<length(VDS)-2)
   up=up+1;
   end

   voh(count)=-VDS(1,VOUTT(up));
   vil(count)=VGS(up)+vdd;
```

```
   down=y2;
   while(down>1 && AveSlope(down, count)<-1 )
   down=down-1;
   end

   vol(count)=-VDS(1,VOUTT(down));
   vih(count)=VGS(down)+vdd;

   NMH(count)= voh(count)-vih(count);
   NML(count)=vil(count)-vol(count);
end


   end
title('Inverter Transfer Curves for Diode Load Delta Vt');
figure
plot(VTl,NMH, 'r')
hold on
plot(VTl,NML, 'b')
title('Noise Magins (red = NMH, blue = NML, set to zero if |max(slope)| < 1)');
xlabel('Vt of load');
ylabel('Volts');

VTdstart = VTdstart - 1.5;
end
%
```

Appendix C: Detailed Process Flows

Standard Single V_T Process

Step	Tool	Notes
Piranha clean	Acid hood	Immerse for 10 minutes in 3:1 sulfuric acid to hydrogen peroxide. Follow with DI rinse and SRD.
Deposit Cr/Au	Ebeam Au	Deposit 100A Cr, 600A Au
Gate photolitography	Coater/EV1	Spin-cast OCG: 5 seconds at 500 RPM, 5 seconds at 750 RPM, 30 seconds at 3000 RPM. Pre-bake 20 minutes at 95°C. Expose 1.6 seconds. Develop 1:30 minutes followed with SRD.
Etch Cr/Au	Acid hood	Immerse and agitate, 5:1 DI water to Transene TFA Au etchant for 1:30 minutes. Rinse in DI water, SRD. Immerse and agitate in 1:1 DI water to CR-7 Cr etchant for 1 minute. Rinse in DI water, SRD.
Photoresist strip	Solvent hood Au	Immerse and agitate in microstrip for 10 minutes. Rinse with DI water, put in DI bubbler for 5 minutes. Put in microstrip for 5 minutes. Rinse with DI water and SRD.
Deposit parylene	Parylene	Lie wafers flat. Weight 0.15 gram parylene-C dimer for 130 nm film.
Via photolithography	Coater/EV1/Var Temp	Spin-cast AZ5214E: 5 seconds at 500 RPM, 5 seconds at 750 RPM, 30 seconds at 2000 RPM. Pre-bake in var temp oven at 88°C for 30 minutes. Expose

		hard contact for 1.4 seconds. Bake in var temp oven at 88°C for 30 minutes. Flood expose for 48 seconds. Develop for 2:20 minutes. Rinse with DI water and SRD.
Reactive ion etch	Plasmaquest	Etch 180 seconds at 100W in O_2.
Photoresist strip	Solvent hood Au	Immerse and agitate in microstrip for 10 minutes. Rinse with DI water, put in DI bubbler for 5 minutes. Put in microstrip for 5 minutes. Rinse with DI water and SRD.
Deposit Au	Ebeam Au or ebeam FP	Deposit 400A Au.
Source/drain photolithography	Coater/EV1	Spin-cast OCG: 5 seconds at 500 RPM, 5 seconds at 750 RPM, 30 seconds at 3000 RPM. Pre-bake 20 minutes at 95°C. Expose 1.6 seconds. Develop 1:30 minutes followed with SRD.
Etch Au	Acid hood	Immerse and agitate, 5:1 DI water to Transene TFA Au etchant for 1:30 minutes. Rinse in DI water, SRD.
Photoresist strip	Solvent hood Au	Immerse and agitate in microstrip for 10 minutes. Rinse with DI water, put in DI bubbler for 5 minutes. Put in microstrip for 5 minutes. Rinse with DI water and SRD.
Check dielectric quality	Sodini Lab	Remove one wafer and check leakage between metal-insulator-metal capacitor.
Deposit pentacene	Pentacene	Pump down to 10^{-6} torr or lower. Measure evaporation rate at 220°C. Evaporate ~10nm of pentacene at ~ 0.8 nm/min. Measure evaporation rate at end.
Deposit parylene	Parylene	Lie wafers flat. Weight 0.15

		gram parylene-C dimer for 130 nm film.
Active photolithography	Coater/EV1	Spin-cast OCG: 5 seconds at 500 RPM, 5 seconds at 750 RPM, 30 seconds at 3000 RPM. Pre-bake 20 minutes at 95°C. Expose 1.6 seconds. Develop 1:30 minutes followed with SRD.
Reactive ion etch	Plasmaquest	Etch 180 seconds at 100W in O_2.

Standard Dual V_T Process

Step	Tool	Notes
Piranha clean	Acid hood	Immerse for 10 minutes in 3:1 sulfuric acid to hydrogen peroxide. Follow with DI rinse and SRD.
High V_T photolithography	Coater/EV1/Var Temp	Spin-cast AZ5214E: 5 seconds at 500 RPM, 5 seconds at 750 RPM, 30 seconds at 2000 RPM. Pre-bake in var temp oven at 88°C for 30 minutes. Expose hard contact for 1.4 seconds. Bake in var temp oven at 88°C for 30 minutes. Flood expose for 48 seconds. Develop for 2:20 minutes. Rinse with DI water and SRD.
Descum	Asher TRL	Ash for 10 minutes at 1000W immediately prior to metal deposition.
Deposit Ti/Pt	Ebeam Au or ebeam FP	Deposit 25 nm Ti, 45 nm Pt at a rate of 1Å/s.
Liftoff	Solvent hood Au	Immerse face down in acetone. Let sit overnight. Replace acetone, and sonicate at power=3 for 3 minutes. Rinse in DI water

		and SRD.
Low V_T photolithography	Coater/EV1/Var Temp	Spin-cast AZ5214E: 5 seconds at 500 RPM, 5 seconds at 750 RPM, 30 seconds at 2000 RPM. Pre-bake in var temp oven at 88°C for 30 minutes. Expose hard contact for 1.4 seconds. Bake in var temp oven at 88°C for 30 minutes. Flood expose for 48 seconds. Develop for 2:20 minutes. Rinse with DI water and SRD.
Descum	Asher TRL	Ash for 10 minutes at 1000W immediately prior to metal deposition.
Deposit Ti/Pt	Ebeam Au or ebeam FP	Deposit 25 nm Ti, 45 nm Pt at a rate of 1Å/s.
Liftoff	Solvent hood Au	Immerse face down in acetone. Let sit overnight. Replace acetone, and sonicate at power=3 for 3 minutes. Rinse in DI water and SRD.
Deposit parylene	Parylene	Lie wafers flat. Weight 0.15 gram parylene-C dimer for 130 nm film.
Via photolithography	Coater/EV1/Var Temp	Spin-cast AZ5214E: 5 seconds at 500 RPM, 5 seconds at 750 RPM, 30 seconds at 2000 RPM. Pre-bake in var temp oven at 88°C for 30 minutes. Expose hard contact for 1.4 seconds. Bake in var temp oven at 88°C for 30 minutes. Flood expose for 48 seconds. Develop for 2:20 minutes. Rinse with DI water and SRD.
Reactive ion etch	Plasmaquest	Etch 180 seconds at 100W in O_2.
Photoresist strip	Solvent hood Au	Immerse and agitate in microstrip for 10 minutes.

		Rinse with DI water, put in DI bubbler for 5 minutes. Put in microstrip for 5 minutes. Rinse with DI water and SRD.
Deposit Au	Ebeam Au or ebeam FP	Deposit 400A Au.
Source/drain photolithography	Coater/EV1	Spin-cast OCG: 5 seconds at 500 RPM, 5 seconds at 750 RPM, 30 seconds at 3000 RPM. Pre-bake 20 minutes at 95°C. Expose 1.6 seconds. Develop 1:30 minutes followed with SRD.
Etch Au	Acid hood	Immerse and agitate, 5:1 DI water to Transene TFA Au etchant for 1:30 minutes. Rinse in DI water, SRD.
Photoresist strip	Solvent hood Au	Immerse and agitate in microstrip for 10 minutes. Rinse with DI water, put in DI bubbler for 5 minutes. Put in microstrip for 5 minutes. Rinse with DI water and SRD.
Check dielectric quality	Sodini Lab	Remove one wafer and check leakage between metal-insulator-metal capacitor.
Deposit pentacene	Pentacene	Pump down to 10^{-6} torr or lower. Measure evaporation rate at 220°C. Evaporate ~10nm of pentacene at ~ 0.8 nm/min. Measure evaporation rate at end.
Deposit parylene	Parylene	Lie wafers flat. Weight 0.15 gram parylene-C dimer for 130 nm film.
Active photolithography	Coater/EV1	Spin-cast OCG: 5 seconds at 500 RPM, 5 seconds at 750 RPM, 30 seconds at 3000 RPM. Pre-bake 20 minutes at 95°C. Expose 1.6 seconds. Develop 1:30 minutes followed with SRD.
Reactive ion etch	Plasmaquest	Etch 180 seconds at 100W in O_2.